



# 3 V to 5 V Single Supply, 200 kSPS 12-Bit Sampling ADC

## AD7853/AD7853L\*

### FEATURES

Specified for  $V_{DD}$  of 3 V to 5 V

Read-Only Operation

AD7853–200 kSPS; AD7853L–100 kSPS

System and Self-Calibration with Autocalibration on Power-Up

Low Power:

AD7853: 15 mW ( $V_{DD} = 3$  V)

AD7853L: 5.5 mW ( $V_{DD} = 3$  V)

Automatic Power Down After Conversion (25  $\mu$ W)

Flexible Serial Interface:

8051/SPI/QSPI/ $\mu$ P Compatible

24-Pin DIP, SOIC and SSOP Packages

### APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants,  
Medical Instruments, Mobile Communications)

Pen Computers

Instrumentation and Control Systems

High Speed Modems

### GENERAL DESCRIPTION

The AD7853/AD7853L are high speed, low power, 12-bit ADCs that operate from a single 3 V or 5 V power supply, the AD7853 being optimized for speed and the AD7853L for low power. The ADC powers up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system-calibration options to ensure accurate operation over time and temperature and have a number of power-down options for low power applications. The part powers up with a set of default conditions and can operate as a read only ADC.

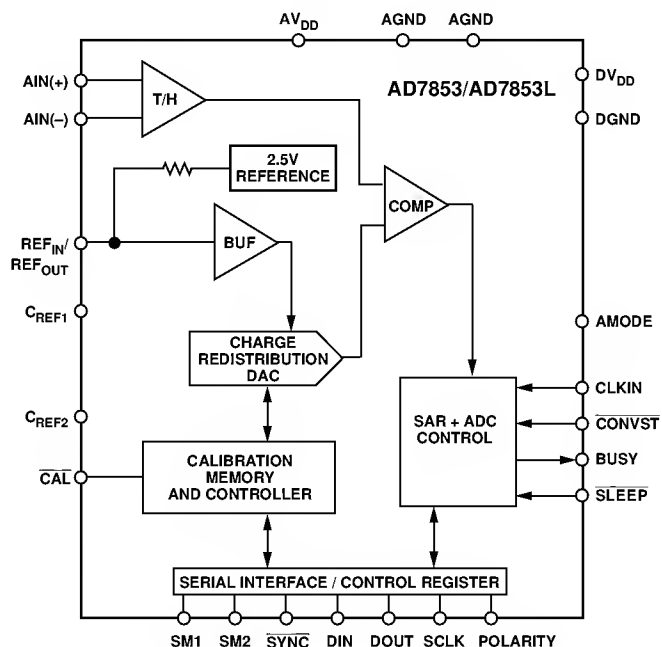
The AD7853 is capable of 200 kHz throughput rate while the AD7853L is capable of 100 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7853/AD7853L voltage range is 0 to  $V_{REF}$  with both straight binary and 2s complement output coding. Input signal range is to the supply, and the part is capable of converting full power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6  $\mu$ W in power-down mode. The part is available in 24-pin, 0.3 inch wide dual-in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.

\*Patent pending.

See Page 35 for data sheet index.

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT HIGHLIGHTS

1. Specified for 3 V and 5 V supplies.
2. Automatic calibration on power-up.
3. Flexible power management options including automatic power-down after conversion.
4. Operates with reference voltages from 1.2 V to  $V_{DD}$ .
5. Analog input ranges from 0 V to  $V_{DD}$ .
6. Self and system calibration.
7. Versatile serial I/O port (SPI/QSPI/8051/ $\mu$ P).
8. Lower power version AD7853L.

### REV. A

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# AD7853/AD7853L—SPECIFICATIONS<sup>1, 2</sup>

( $AV_{DD} = DV_{DD} = +3.0\text{ V to }+5.5\text{ V}$ ,  $REF_{IN}/REF_{OUT} = 2.5\text{ V}$  External Reference,  $f_{CLKIN} = 4\text{ MHz}$  (1.8 MHz B Grade ( $0^{\circ}\text{C to }+70^{\circ}\text{C}$ ), 1 MHz A and B Grades ( $-40^{\circ}\text{C to }+85^{\circ}\text{C}$ ) for L Version);  $f_{SAMPLE} = 200\text{ kHz}$  (AD7853) 100 kHz (AD7853L); SLEEP = Logic High;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.) Specifications in ( ) apply to the AD7853L.

Parameter	A Version <sup>1</sup>	B Version <sup>1</sup>	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio <sup>3</sup> (SNR)	70	71	dB min	Typically SNR is 72 dB V <sub>IN</sub> = 10 kHz Sine Wave, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Total Harmonic Distortion (THD)	-78	-78	dB max	V <sub>IN</sub> = 10 kHz Sine Wave, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Peak Harmonic or Spurious Noise Intermodulation Distortion (IMD)	-78	-78	dB max	V <sub>IN</sub> = 10 kHz Sine Wave, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Second Order Terms	-78	-80	dB typ	f <sub>a</sub> = 9.983 kHz, f <sub>b</sub> = 10.05 kHz, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
Third Order Terms	-78	-80	dB typ	f <sub>a</sub> = 9.983 kHz, f <sub>b</sub> = 10.05 kHz, f <sub>SAMPLE</sub> = 200 kHz (100 kHz)
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1	LSB max	2.5 V External Reference V <sub>DD</sub> = 3 V, V <sub>DD</sub> = 5 V (B Grade Only)
	±1	±0.5	LSB max	5 V External Reference V <sub>DD</sub> = 5 V
		(±1)	LSB max	(L Version, 5 V External Reference, V <sub>DD</sub> = 5 V)
	(±1)		LSB max	(L Version)
Differential Nonlinearity	±1	±1	LSB max	Guaranteed No Missed Codes to 12 Bits. 2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V
Total Unadjusted Error	±1	±1	LSB typ	
Unipolar Offset Error	±1	±1	LSB max	2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V
Unipolar Offset Error	(±2.5)	(±2.5)	LSB max	(L Versions, 2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V)
Positive Full-Scale Error	±2.5	±2.5	LSB max	2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V
Positive Full-Scale Error	(±4)	(±4)	LSB max	(L Versions, 2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V)
Negative Full-Scale Error	±2.5	±2.5	LSB max	2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V
Negative Full-Scale Error	(±4)	(±4)	LSB max	(L Versions, 2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V)
Bipolar Zero Error	±2	±2	LSB max	2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V
Bipolar Zero Error	(±2.5)	(±2.5)	LSB max	(L Versions, 2.5 V External Reference V <sub>DD</sub> = 3 V, 5 V External Reference V <sub>DD</sub> = 5 V)
ANALOG INPUT				
Input Voltage Ranges	0 to V <sub>REF</sub>	0 to V <sub>REF</sub>	Volts	i.e., AIN(+) – AIN(–) = 0 to V <sub>REF</sub> , AIN(–) can be biased up but AIN(+) cannot go below AIN(–)
	±V <sub>REF</sub> /2	±V <sub>REF</sub> /2	Volts	i.e., AIN(+) – AIN(–) = –V <sub>REF</sub> /2 to +V <sub>REF</sub> /2, AIN(–) should be biased to +V <sub>REF</sub> /2 and AIN(+) can go below AIN(–) but cannot go below 0 V
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF <sub>IN</sub> Input Voltage Range	2.3/V <sub>DD</sub>	2.3/V <sub>DD</sub>	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	
REF <sub>OUT</sub> Output Voltage	2.3/2.7	2.3/2.7	V min/max	
REF <sub>OUT</sub> Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V <sub>INH</sub>	2.4	2.4	V min	AV <sub>DD</sub> = DV <sub>DD</sub> = 4.5 V to 5.5 V
	2.1	2.1	V min	AV <sub>DD</sub> = DV <sub>DD</sub> = 3.0 V to 3.6 V
Input Low Voltage, V <sub>INL</sub>	0.8	0.8	V max	AV <sub>DD</sub> = DV <sub>DD</sub> = 4.5 V to 5.5 V
	0.6	0.6	V max	AV <sub>DD</sub> = DV <sub>DD</sub> = 3.0 V to 3.6 V
Input Current, I <sub>IN</sub>	±10	±10	µA max	Typically 10 nA, V <sub>IN</sub> = 0 V or V <sub>DD</sub>
Input Capacitance, C <sub>IN</sub> <sup>4</sup>	10	10	pF max	

Parameter	A Version <sup>1</sup>	B Version <sup>1</sup>	Units	Test Conditions/Comments
<b>LOGIC OUTPUTS</b>				
Output High Voltage, $V_{OH}$	4	4	V min	$I_{SOURCE} = 200 \mu A$ $AV_{DD} = DV_{DD} = 4.5 V$ to $5.5 V$
	2.4	2.4	V min	$AV_{DD} = DV_{DD} = 3.0 V$ to $3.6 V$
Output Low Voltage, $V_{OL}$	0.4	0.4	V max	$I_{SINK} = 0.8 mA$
Floating-State Leakage Current	$\pm 10$	$\pm 10$	$\mu A$ max	
Floating-State Output Capacitance <sup>4</sup>	10	10	pF max	
Output Coding	Straight (Natural) Binary			Unipolar Input Range
	2s Complement			Bipolar Input Range
<b>CONVERSION RATE</b>				
Conversion Time	4.6 (18)	4.6 (18)	$\mu s$ max	(L Versions Only, $-40^{\circ}C$ to $+85^{\circ}C$ , 1 MHz CLKIN)
		(10)	$\mu s$ max	(L Versions Only, $0^{\circ}C$ to $+70^{\circ}C$ , 1.8 MHz CLKIN)
Track/Hold Acquisition Time	0.4 (1)	0.4 (1)	$\mu s$ min	(L Versions Only)
<b>POWER REQUIREMENTS</b>				
$AV_{DD}, DV_{DD}$	+3.0/+5.5	+3.0/+5.5	V min/max	
$I_{DD}$				
Normal Mode <sup>5</sup>	6 (1.9)	6 (1.9)	mA max	$AV_{DD} = DV_{DD} = 4.5 V$ to $5.5 V$ . Typically 4.5 mA (1.5);
	5.5 (1.9)	5.5 (1.9)	mA max	$AV_{DD} = DV_{DD} = 3.0 V$ to $3.6 V$ . Typically 4.0 mA (1.5 mA)
Sleep Mode <sup>6</sup>				
With External Clock On	10	10	$\mu A$ typ	Full power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	400	400	$\mu A$ typ	Partial power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
With External Clock Off	5	5	$\mu A$ max	Typically 1 $\mu A$ . Full power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	200	200	$\mu A$ typ	Partial Power Down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
Normal Mode Power Dissipation	33 (10.5)	33 (10.5)	mW max	$V_{DD} = 5.5 V$ : Typically 25 mW (8); $\overline{SLEEP} = V_{DD}$
	20 (6.85)	20 (6.85)	mW max	$V_{DD} = 3.6 V$ : Typically 15 mW (5.4); $\overline{SLEEP} = V_{DD}$
Sleep Mode Power Dissipation				
With External Clock On	55	55	$\mu W$ typ	$V_{DD} = 5.5 V$ ; $\overline{SLEEP} = 0 V$
	36	36	$\mu W$ typ	$V_{DD} = 3.6 V$ ; $\overline{SLEEP} = 0 V$
With External Clock Off	27.5	27.5	$\mu W$ max	$V_{DD} = 5.5 V$ : Typically 5.5 $\mu W$ ; $\overline{SLEEP} = 0 V$
	18	18	$\mu W$ max	$V_{DD} = 3.6 V$ : Typically 3.6 $\mu W$ ; $\overline{SLEEP} = 0 V$
<b>SYSTEM CALIBRATION</b>				
Offset Calibration Span <sup>7</sup>	$+0.05 \times V_{REF}/-0.05 \times V_{REF}$		V max/min	Allowable Offset Voltage Span for Calibration
Gain Calibration Span <sup>7</sup>	$+1.025 \times V_{REF}/-0.975 \times V_{REF}$		V max/min	Allowable Full-Scale Voltage Span for Calibration

## NOTES

<sup>1</sup>Temperature ranges as follows: A, B Versions,  $-40^{\circ}C$  to  $+85^{\circ}C$ . For L Versions, A and B Versions  $f_{CLKIN} = 1 MHz$  over  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range,

B Version  $f_{CLKIN} = 1.8 MHz$  over  $0^{\circ}C$  to  $+70^{\circ}C$  temperature range.

<sup>2</sup>Specifications apply after calibration.

<sup>3</sup>SNR calculation includes distortion and noise components.

<sup>4</sup>Sample tested @  $+25^{\circ}C$  to ensure compliance.

<sup>5</sup>All digital inputs @ DGND except for CONVST,  $\overline{SLEEP}$ ,  $\overline{CAL}$ , and  $\overline{SYNC}$  @  $DV_{DD}$ . No load on the digital outputs. Analog inputs @ AGND.

<sup>6</sup>CLKIN @ DGND when external clock off. All digital inputs @ DGND except for CONVST,  $\overline{SLEEP}$ ,  $\overline{CAL}$ , and  $\overline{SYNC}$  @  $DV_{DD}$ . No load on the digital outputs. Analog inputs @ AGND.

<sup>7</sup>The offset and gain calibration spans are defined as the range of offset and gain errors that the AD7853/AD7853L can calibrate. Note also that these are voltage spans and are not absolute voltages (i.e., the allowable system offset voltage presented at AIN(+) for the system offset error to be adjusted out will be  $AIN(-) \pm 0.05 \times V_{REF}$ , and the allowable system full-scale voltage applied between AIN(+) and AIN(-) for the system full-scale voltage error to be adjusted out will be  $V_{REF} \pm 0.025 \times V_{REF}$ ). This is explained in more detail in the calibration section of the data sheet.

Specifications subject to change without notice.

# AD7853/AD7853L

## TIMING SPECIFICATIONS<sup>1</sup> ( $AV_{DD} = DV_{DD} = +3.0\text{ V to }+5.5\text{ V}$ ; $f_{CLKIN} = 4\text{ MHz}$ for AD7853 and 1.8/1 MHz for AD7853L; $T_A = T_{MIN}$ to $T_{MAX}$ , unless otherwise noted)

Parameter	Limit at $T_{MIN}$ , $T_{MAX}$ (A, B Versions)		Units	Description
	5 V	3 V		
$f_{CLKIN}$ <sup>2</sup>	500 4 1.8 1	500 4 1.8 1	kHz min MHz max MHz max MHz max	Master Clock Frequency  L Version, 0°C to +70°C, B Grade Only L Version, -40°C to +85°C
$f_{SCLK}$ <sup>3</sup>	4 $f_{CLKIN}$	4 $f_{CLKIN}$	MHz max MHz max	Interface Modes 1, 2, 3 (External Serial Clock) Interface Modes 4, 5 (Internal Serial Clock)
$t_1$ <sup>4</sup>	100	100	ns min	CONVST Pulse Width
$t_2$	50	90	ns max	CONVST↓ to BUSY↑ Propagation Delay
$t_{CONVERT}$	4.6 10 (18)	4.6 10 (18)	μs max μs max	Conversion Time = $18\ t_{CLKIN}$ L Version 1.8 (1) MHz CLKIN. Conversion Time = $18\ t_{CLKIN}$
$t_3$	-0.4 $t_{SCLK}$ $\mp 0.4\ t_{SCLK}$	-0.4 $t_{SCLK}$ $\mp 0.4\ t_{SCLK}$	ns min ns min/max	SYNC↓ to SCLK↓ Setup Time (Noncontinuous SCLK Input) SYNC↓ to SCLK↓ Setup Time (Continuous SCLK Input)
$t_4$	0.6 $t_{SCLK}$	0.6 $t_{SCLK}$	ns min	SYNC↓ to SCLK↓ Setup Time. Interface Mode 4 Only
$t_5$ <sup>5</sup>	50	90	ns max	Delay from SYNC↓ until DOUT 3-State Disabled
$t_{5A}$ <sup>5</sup>	50	90	ns max	Delay from SYNC↓ until DIN 3-State Disabled
$t_6$ <sup>5</sup>	75	115	ns max	Data Access Time After SCLK↓
$t_7$	40	60	ns min	Data Setup Time Prior to SCLK↑
$t_8$	20	30	ns min	Data Valid to SCLK Hold Time
$t_9$ <sup>6</sup>	0.4 $t_{SCLK}$	0.4 $t_{SCLK}$	ns min	SCLK High Pulse Width (Interface Modes 4 and 5)
$t_{10}$ <sup>6</sup>	0.4 $t_{SCLK}$	0.4 $t_{SCLK}$	ns min	SCLK Low Pulse Width (Interface Modes 4 and 5)
$t_{11}$	30 30/0.4 $t_{SCLK}$	50 50/0.4 $t_{SCLK}$	ns min ns min/max	SCLK↑ to SYNC↑ Hold Time (Noncontinuous SCLK) (Continuous SCLK) Does Not Apply to Interface Mode 3
$t_{11A}$	50	50	ns max	SCLK↑ to SYNC↑ Hold Time
$t_{12}$ <sup>7</sup>	50	50	ns max	Delay from SYNC↑ until DOUT 3-State Enabled
$t_{13}$	90	130	ns max	Delay from SCLK↑ to DIN Being Configured as Output
$t_{14}$ <sup>8</sup>	50	90	ns max	Delay from SCLK↑ to DIN Being Configured as Input
$t_{15}$	2.5 $t_{CLKIN}$	2.5 $t_{CLKIN}$	ns max	CAL↑ to BUSY↑ Delay
$t_{16}$	2.5 $t_{CLKIN}$	2.5 $t_{CLKIN}$	ns max	CONVST↓ to BUSY↑ Delay in Calibration Sequence
$t_{CAL}$ <sup>9</sup>	31.25	31.25	ms typ	Full Self-Calibration Time, Master Clock Dependent ( $125013\ t_{CLKIN}$ )
$t_{CAL1}$ <sup>9</sup>	27.78	27.78	ms typ	Internal DAC Plus System Full-Scale Cal Time, Master Clock Dependent ( $111114\ t_{CLKIN}$ )
$t_{CAL2}$ <sup>9</sup>	3.47	3.47	ms typ	System Offset Calibration Time, Master Clock Dependent ( $13899\ t_{CLKIN}$ )

### NOTES

Descriptions that refer to SCLK↑ (rising) or SCLK↓ (falling) edges here are with the POLARITY pin HIGH. For the POLARITY pin LOW then the opposite edge of SCLK will apply.

<sup>1</sup>Sample tested at +25°C to ensure compliance. All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of 1.6 V. See

Table XI and timing diagrams for different interface modes and calibration.

<sup>2</sup>Mark/Space ratio for the master clock input is 40/60 to 60/40.

<sup>3</sup>For Interface Modes 1, 2, 3 the SCLK max frequency will be 4 MHz. For Interface Modes 4 and 5 the SCLK will be an output and the frequency will be  $f_{CLKIN}$ .

<sup>4</sup>The CONVST pulse width will here only apply for normal operation. When the part is in power-down mode, a different CONVST pulse width will apply (see Power-Down section).

<sup>5</sup>Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

<sup>6</sup>For self-clocking mode (Interface Modes 4, 5) the nominal SCLK high and low times will be  $0.5\ t_{SCLK} = 0.5\ t_{CLKIN}$ .

<sup>7</sup> $t_{12}$  is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time,  $t_{12}$ , quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

<sup>8</sup> $t_{14}$  is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the timing characteristics is the true delay of the part in turning off the output drivers and configuring the DIN line as an input. Once this time has elapsed the user can drive the DIN line knowing that a bus conflict will not occur.

<sup>9</sup>The typical time specified for the calibration times is for a master clock of 4 MHz. For the L version the calibration times will be longer than those quoted here due to the 1.8/1 MHz master clock.

Specifications subject to change without notice.

## TYPICAL TIMING DIAGRAMS

Figures 2 and 3 show typical read and write timing diagrams. Figure 2 shows the reading and writing after conversion in Interface Modes 2 and 3. To attain the maximum sample rate of 100 kHz (AD7853L) or 200 kHz (AD7853) in Interface Modes 2 and 3, reading and writing must be performed during conversion. Figure 3 shows the timing diagram for Interface Modes 4 and 5 with sample rate of 100 kHz (AD7853L) or 200 kHz (AD7853). At least 400 ns acquisition time must be allowed (the time from the falling edge of BUSY to the next rising edge of CONVST) before the next conversion begins to ensure that the part is settled to the 12-bit level. If the user does not want to provide the CONVST signal, the conversion can be initiated in software by writing to the control register.

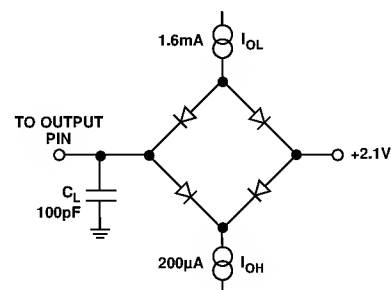


Figure 1. Load Circuit for Digital Output Timing Specifications

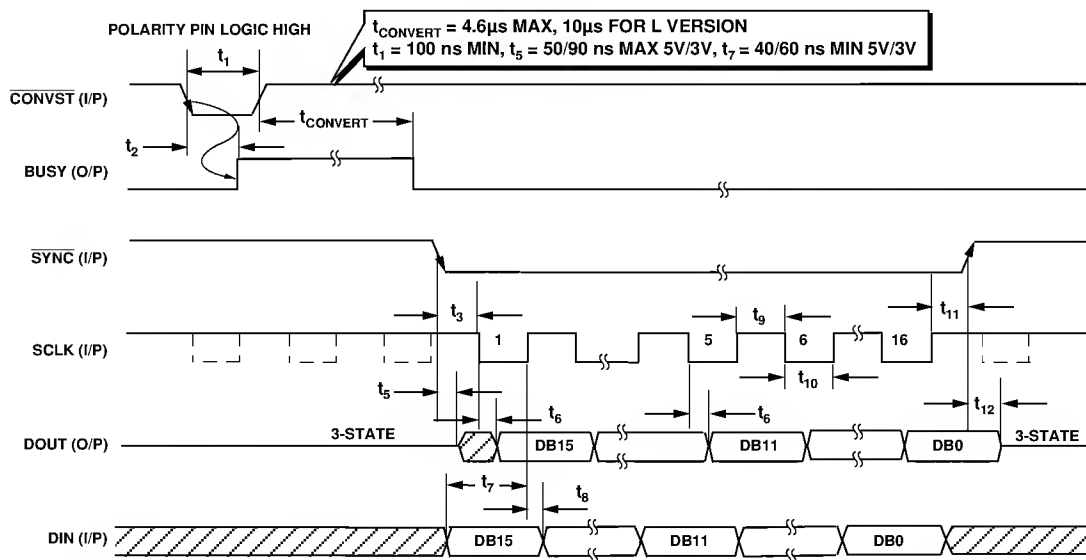


Figure 2. AD7853/AD7853L Timing Diagram (Typical Read and Write Operation for Interface Modes 2, 3)

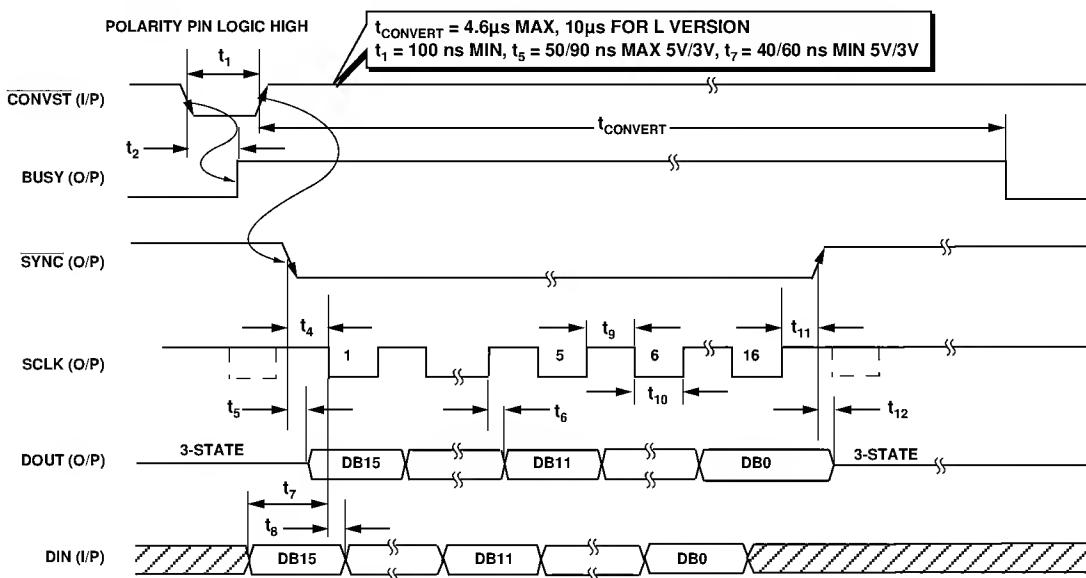


Figure 3. AD7853/AD7853L Timing Diagram (Typical Read and Write Operation for Interface Modes 4, 5)

# AD7853/AD7853L

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

AV <sub>DD</sub> to AGND	−0.3 V to +7 V
DV <sub>DD</sub> to DGND	−0.3 V to +7 V
AV <sub>DD</sub> to DV <sub>DD</sub>	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV <sub>DD</sub> + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV <sub>DD</sub> + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV <sub>DD</sub> + 0.3 V
REF <sub>IN</sub> /REF <sub>OUT</sub> to AGND	−0.3 V to AV <sub>DD</sub> + 0.3 V
Input Current to Any Pin Except Supplies <sup>2</sup>	±10 mA
Operating Temperature Range	
Commercial (A, B Versions)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Plastic DIP Package, Power Dissipation	450 mW
θ <sub>JA</sub> Thermal Impedance	105°C/W
θ <sub>JC</sub> Thermal Impedance	34.7°C/W
Lead Temperature, (Soldering, 10 secs)	+260°C
SOIC, SSOP Package, Power Dissipation	450 mW
θ <sub>JA</sub> Thermal Impedance	75°C/W (SOIC) 115°C/W (SSOP)
θ <sub>JC</sub> Thermal Impedance	25°C/W (SOIC) 35°C/W (SSOP)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infrared (15 secs)	+220°C
ESD	>3 kV

## NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Transient currents of up to 100 mA will not cause SCR latch up.

## ORDERING GUIDE

Model	Linearity Error (LSB) <sup>1</sup>	Power Dissipation (mW)	Package Option <sup>2</sup>
AD7853AN	±1	20	N-24
AD7853BN	±1/2	20	N-24
AD7853LAN <sup>3</sup>	±1	6.85	N-24
AD7853LBN <sup>3</sup>	±1	6.85	N-24
AD7853AR	±1	20	R-24
AD7853BR	±1/2	20	R-24
AD7853LAR <sup>3</sup>	±1	6.85	R-24
AD7853LBR <sup>3</sup>	±1	6.85	R-24
AD7853LARS <sup>3</sup>	±1	6.85	RS-24
EVAL-AD7853CB <sup>4</sup>			
EVAL-CONTROL BOARD <sup>5</sup>			

## NOTES

<sup>1</sup>Linearity error refers to the integral linearity error.

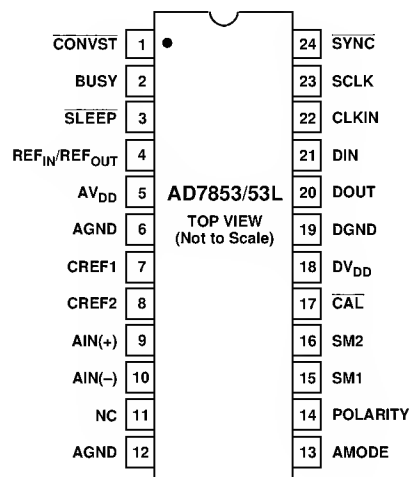
<sup>2</sup>N = Plastic DIP; R = SOIC; RS = SSOP.

<sup>3</sup>L signifies the low power version.

<sup>4</sup>This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

<sup>5</sup>This board is a complete unit allowing a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designators.

## PINOUTS FOR DIP, SOIC AND SSOP



## TERMINOLOGY

### Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

### Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

### Total Unadjusted Error

This is the deviation of the actual code from the ideal code taking all errors into account (*Gain, Offset, Integral Nonlinearity, and other errors*) at any point along the transfer function.

### Unipolar Offset Error

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(−) + 1/2 LSB) when operating in the unipolar mode.

### Positive Full-Scale Error

This applies to the unipolar and bipolar modes and is the deviation of the last code transition from the ideal AIN(+) voltage (AIN(−) + Full Scale − 1.5 LSB) after the offset error has been adjusted out.

### Negative Full-Scale Error

This applies to the bipolar mode only and is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(−) − V<sub>REF</sub>/2 + 0.5 LSB).

### Bipolar Zero Error

This is the deviation of the midscale transition (all 0s to all 1s) from the ideal AIN(+) voltage (AIN(−) − 1/2 LSB).

### Track/Hold Acquisition Time

The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ± 1/2 LSB, after the end of conversion.

### Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f<sub>s</sub>/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB.

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7853/AD7853L, it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V<sub>1</sub> is the rms amplitude of the fundamental and V<sub>2</sub>, V<sub>3</sub>, V<sub>4</sub>, V<sub>5</sub> and V<sub>6</sub> are the rms amplitudes of the second through the sixth harmonics.

### Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f<sub>s</sub>/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

### Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f<sub>a</sub> and f<sub>b</sub>, any active device with nonlinearities will create distortion products at sum and difference frequencies of m f<sub>a</sub> ± n f<sub>b</sub> where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (f<sub>a</sub> + f<sub>b</sub>) and (f<sub>a</sub> − f<sub>b</sub>), while the third order terms include (2f<sub>a</sub> + f<sub>b</sub>), (2f<sub>a</sub> − f<sub>b</sub>), (f<sub>a</sub> + 2f<sub>b</sub>) and (f<sub>a</sub> − 2f<sub>b</sub>).

Testing is performed using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

# AD7853/AD7853L

## AD7853/AD7853L PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert Start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. When this input is not used, it should be tied to $\text{DV}_{\text{DD}}$ .
2	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ or rising edge of $\overline{\text{CAL}}$ , and remains high until conversion is completed. BUSY is also used to indicate when the AD7853/AD7853L has completed its on-chip calibration sequence.
3	$\overline{\text{SLEEP}}$	Sleep Input/Low Power Mode. A logic 0 initiates a sleep and all circuitry is powered down including the internal voltage reference provided there is no conversion or calibration being performed. Calibration data is retained. A logic 1 results in normal operation. See Power-Down section for more details.
4	$\text{REF}_{\text{IN}}/\text{REF}_{\text{OUT}}$	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal reference voltage is 2.5 V and this appears at the pin. This pin can be overdriven by an external reference or can be taken as high as $\text{AV}_{\text{DD}}$ . When this pin is tied to $\text{AV}_{\text{DD}}$ , then the $\text{C}_{\text{REF1}}$ pin should also be tied to $\text{AV}_{\text{DD}}$ .
5	$\text{AV}_{\text{DD}}$	Analog Positive Supply Voltage, +3.0 V to +5.5 V.
6, 12	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
7	$\text{C}_{\text{REF1}}$	Reference Capacitor (0.1 $\mu\text{F}$ multilayer ceramic). This external capacitor is used as a charge source for the internal DAC. The capacitor should be tied between the pin and AGND.
8	$\text{C}_{\text{REF2}}$	Reference Capacitor (0.01 $\mu\text{F}$ ceramic disc). This external capacitor is used in conjunction with the on-chip reference. The capacitor should be tied between the pin and AGND.
9	$\text{AIN}(+)$	Analog Input. Positive input of the pseudo-differential analog input. Cannot go below AGND or above $\text{AV}_{\text{DD}}$ at any time, and cannot go below $\text{AIN}(-)$ when the unipolar input range is selected.
10	$\text{AIN}(-)$	Analog Input. Negative input of the pseudo-differential analog input. Cannot go below AGND or above $\text{AV}_{\text{DD}}$ at any time.
11	NC	No Connect Pin.
13	AMODE	Analog Mode Pin. This pin allows two different analog input ranges to be selected. A logic 0 selects range 0 to $\text{V}_{\text{REF}}$ (i.e., $\text{AIN}(+) - \text{AIN}(-) = 0$ to $\text{V}_{\text{REF}}$ ). In this case $\text{AIN}(+)$ cannot go below $\text{AIN}(-)$ and $\text{AIN}(-)$ cannot go below AGND. A logic 1 selects range $-\text{V}_{\text{REF}}/2$ to $+\text{V}_{\text{REF}}/2$ (i.e., $\text{AIN}(+) - \text{AIN}(-) = -\text{V}_{\text{REF}}/2$ to $+\text{V}_{\text{REF}}/2$ ). In this case $\text{AIN}(+)$ cannot go below AGND so that $\text{AIN}(-)$ needs to be biased to $+\text{V}_{\text{REF}}/2$ to allow $\text{AIN}(+)$ to go from 0 V to $+\text{V}_{\text{REF}}$ V.
14	POLARITY	Serial Clock Polarity. This pin determines the active edge of the serial clock (SCLK). Toggling this pin will reverse the active edge of the serial clock (SCLK). A logic 1 means that the serial clock (SCLK) idles high and a logic 0 means that the serial clock (SCLK) idles low. It is best to refer to the timing diagrams and Table X for the SCLK active edges.
15	SM1	Serial Mode Select Pin. This pin is used in conjunction with the SM2 pin to give different modes of operation as described in Table XI.
16	SM2	Serial Mode Select Pin. This pin is used in conjunction with the SM1 pin to give different modes of operation as described in Table XI.
17	$\overline{\text{CAL}}$	Calibration Input. This pin has an internal pull-up current source of 0.15 $\mu\text{A}$ . A logic 0 on this pin resets all logic and initiates a calibration on its rising edge. There is the option of connecting a 10 nF capacitor from this pin to AGND to allow for an automatic self calibration on power-up. This input overrides all other internal operations.
18	$\text{DV}_{\text{DD}}$	Digital Supply Voltage, +3.0 V to +5.5 V.
19	DGND	Digital Ground. Ground reference point for digital circuitry.
20	DOUT	Serial Data Output. The data output is supplied to this pin as a 16-bit serial word.
21	DIN	Serial Data Input. The data to be written is applied to this pin in serial form (16-bit word). This pin can act as an input pin or as a I/O pin depending on the serial interface mode the part is in (see Table XI).
22	CLKIN	Master Clock Signal for the device (4 MHz for AD7853, 1.8 MHz for AD7853L). Sets the conversion and calibration times.
23	SCLK	Serial Port Clock. Logic input/output. The SCLK pin is configured as an input or output, dependent on the type of serial data transmission (self-clocking or external-clocking) that has been selected by the SM1 and SM2 pins. The SCLK idles high or low depending on the state of the POLARITY pin.
24	$\overline{\text{SYNC}}$	This pin can be an input level triggered active low (similar to a chip select in one case and to a frame sync in the other) or an output (similar to a frame sync) pin depending on SM1, SM2 (see Table XI).



## AD7853/AD7853L ON-CHIP REGISTERS

The AD7853/AD7853L powers up with a set of default conditions, and the user need not ever write to the device. In this case the AD7853/AD7853L will operate as a Read-Only ADC. The AD7853/AD7853L still retains the flexibility for performing a full power-down, and a full self-calibration. Note that the DIN pin should be tied to DGND for operating the AD7853/AD7853L as a Read-Only ADC.

Extra features and flexibility such as performing different power-down options, different types of calibrations including system calibration, and software conversion start can be selected by writing to the part.

The AD7853/AD7853L contains a **Control register**, **ADC output data register**, **Status register**, **Test register** and **10 Calibration registers**. The control register is write-only, the ADC output data register and the status register are read-only, and the test and calibration registers are both read/write registers. The test register is used for testing the part and should not be written to.

### Addressing the On-Chip Registers

#### Writing

A write operation to the AD7853/AD7853L consists of 16 bits. The two MSBs, ADDR0 and ADDR1, are decoded to determine which register is addressed, and the subsequent 14 bits of data are written to the addressed register. It is not until all 16 bits are written that the data is latched into the addressed register. Table I shows the decoding of the address bits, while Figure 4 shows the overall write register hierarchy.

Table I. Write Register Addressing

ADDR1	ADDR0	Comment
0	0	This combination does not address any register so the subsequent 14 data bits are ignored.
0	1	This combination addresses the <b>TEST REGISTER</b> . The subsequent 14 data bits are written to the test register.
1	0	This combination addresses the <b>CALIBRATION REGISTERS</b> . The subsequent 14 data bits are written to the selected calibration register.
1	1	This combination addresses the <b>CONTROL REGISTER</b> . The subsequent 14 data bits are written to the control register.

#### Reading

To read from the various registers the user must first write to Bits 6 and 7 in the Control Register, RDSLT0 and RDSLT1. These bits are decoded to determine which register is addressed during a read operation. Table II shows the decoding of the read address bits while Figure 5 shows the overall read register hierarchy. The power-up status of these bits is 00 so that the default read will be from the ADC output data register.

Once the read selection bits are set in the control register all subsequent read operations that follow will be from the selected register until the read selection bits are changed in the control register.

Table II. Read Register Addressing

RDSLT1	RDSLT0	Comment
0	0	All successive read operations will be from <b>ADC OUTPUT DATA REGISTER</b> . This is the power-up default setting. There will always be four leading zeros when reading from the ADC output data register.
0	1	All successive read operations will be from <b>TEST REGISTER</b> .
1	0	All successive read operations will be from <b>CALIBRATION REGISTERS</b> .
1	1	All successive read operations will be from <b>STATUS REGISTER</b> .

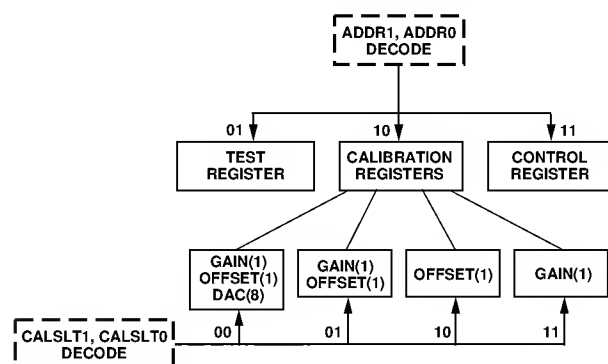


Figure 4. Write Register Hierarchy/Address Decoding

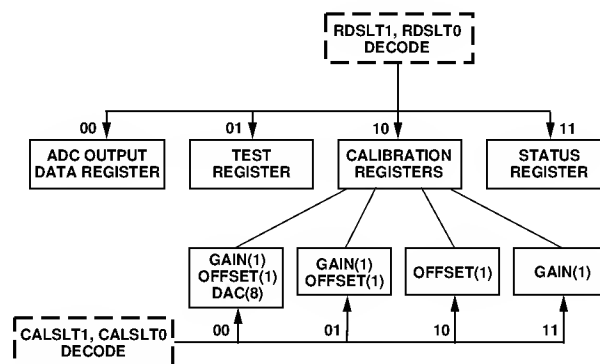


Figure 5. Read Register Hierarchy/Address Decoding

# AD7853/AD7853L

## CONTROL REGISTER

The arrangement of the control register is shown below. The control register is a write only register and contains 14 bits of data. The control register is selected by putting two 1s in ADDR1 and ADDR0. The function of the bits in the control register are described below. The power-up status of all bits is 0.

MSB

ZERO	ZERO	ZERO	ZERO	PMGT1	PMGT0	RDSLT1
RDSLT0	$2/3$ MODE	CONVST	CALMD	CALSLT1	CALSLT0	STCAL

LSB

Control Register Bit Function Description

Bit	Mnemonic	Comment
13	ZERO	These four bits must be set to 0 when writing to the control register.
12	ZERO	
11	ZERO	
10	ZERO	
9	PMGT1	Power Management Bits. These two bits are used with the $\overline{\text{SLEEP}}$ pin for putting the part into various power-down modes (See <i>Power-Down</i> section for more details).
8	PMGT0	
7	RDSLT1	Theses two bits determine which register is addressed for the read operations. See Table II.
6	RDSLT0	
5	$2/3$ MODE	Interface Mode Select Bit. With this bit set to 0, Interface Mode 2 is enabled. With this bit set to 1, Interface Mode 1 is enabled where DIN is used as an output as well as an input. This bit is set to 0 by default after every read cycle; thus when using Interface Mode 1, this bit needs to be set to 1 in every write cycle.
4	CONVST	Conversion Start Bit. A logic one in this bit position starts a single conversion, and this bit is automatically reset to 0 at the end of conversion. This bit may also used in conjunction with system calibration (see calibration section on page 21).
3	CALMD	Calibration Mode Bit. A 0 here selects self-calibration and a 1 selects a system calibration (see Table III).
2	CALSLT1	Calibration Selection Bits and Start Calibration Bit. These bits have two functions. With the STCAL bit set to 1, the CALSLT1 and CALSLT0 bits determine the type of calibration performed by the part (see Table III). The STCAL bit is automatically reset to 0 at the end of calibration. With the STCAL bit set to 0, the CALSLT1 and CALSLT0 bits are decoded to address the calibration register for read/write of calibration coefficients (see section on the calibration registers for more details).
1	CALSLT0	
0	STCAL	

Table III. Calibration Selection

CALMD	CALSLT1	CALSLT0	Calibration Type
0	0	0	A <b>full internal calibration</b> is initiated where the internal DAC is calibrated followed by the internal gain error and finally the internal offset error is calibrated out. This is the default setting.
0	0	1	Here the <b>internal gain error</b> is calibrated out followed by the <b>internal offset error</b> calibrated out.
0	1	0	This calibrates out the <b>internal offset error</b> only.
0	1	1	This calibrates out the <b>internal gain error</b> only.
1	0	0	A <b>full system calibration</b> is initiated here where first the internal DAC is calibrated, followed by the system gain error, and finally the system offset error is calibrated out.
1	0	1	Here the <b>system gain error</b> is calibrated out followed by the <b>system offset error</b> .
1	1	0	This calibrates out the <b>system offset error</b> only.
1	1	1	This calibrates out the <b>system gain error</b> only.

**STATUS REGISTER**

The arrangement of the status register is shown below. The status register is a read-only register and contains 16 bits of data. The status register is selected by first writing to the control register and putting two 1s in RDSLT1 and RDSLT0. The function of the bits in the status register are described below. The power-up status of all bits is 0.

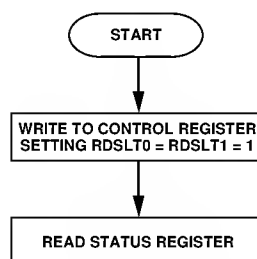


Figure 6. Flowchart for Reading the Status Register

**MSB**

ZERO	BUSY	ZERO	ZERO	ZERO	ZERO	PMGT1	PMGT0
------	------	------	------	------	------	-------	-------

RDSLT1	RDSLT0	2/3 MODE	X	CALMD	CALSLT1	CALSLT0	STCAL
--------	--------	----------	---	-------	---------	---------	-------

**LSB**

**Status Register Bit Function Description**

Bit	Mnemonic	Comment
15	ZERO	This bit is always 0.
14	BUSY	Conversion/Calibration Busy Bit. When this bit is 1, this indicates that there is a conversion or calibration in progress. When this bit is 0, there is no conversion or calibration in progress.
13	ZERO	These four bits are always 0.
12	ZERO	
11	ZERO	
10	ZERO	
9	PMGT1	Power Management Bits. These bits along with the $\overline{\text{SLEEP}}$ pin will indicate if the part is in a power-down mode or not. See Table VI in Power-Down Section for description.
8	PMGT0	
7	ONE	Both these bits are always 1 indicating it is the status register that is being read. See Table II.
6	ONE	
5	2/3 MODE	Interface Mode Select Bit. With this bit 0, the device is in Interface Mode 2. With this bit 1, the device is in Interface Mode 1. This bit is reset to 0 after every read cycle.
4	X	Don't care bit.
3	CALMD	Calibration Mode Bit. A 0 in this bit indicates a self-calibration is selected, and a 1 in this bit indicates a system calibration is selected (see Table III).
2	CALSLT1	Calibration Selection Bits and Start Calibration Bit. The STCAL bit is read as a 1 if a calibration is in progress and as a 0 if there is no calibration in progress. The CALSLT1 and CALSLT0 bits indicate which of the calibration registers are addressed for reading and writing (see section on the Calibration Registers for more details).
1	CALSLT0	
0	STCAL	

# AD7853/AD7853L

## CALIBRATION REGISTERS

The AD7853/AD7853L has 10 calibration registers in all, 8 for the DAC, 1 for the offset and 1 for gain. Data can be written to or read from all 10 calibration registers. In self and system calibration the part automatically modifies the calibration registers; only if the user needs to modify the calibration registers should an attempt be made to read from and write to the calibration registers.

### Addressing the Calibration Registers

The calibration selection bits in the control register CALSLT1 and CALSLT0 determine which of the calibration registers are addressed (See Table IV). The addressing applies to both the read and write operations for the calibration registers. The user should not attempt to read from and write to the calibration registers at the same time.

Table IV. Calibration Register Addressing

CALSLT1	CALSLT0	Comment
0	0	This combination addresses the <b>Gain (1), Offset (1) and DAC Registers (8)</b> . Ten registers in total.
0	1	This combination addresses the <b>Gain (1) and Offset (1)</b> Registers. Two registers in total.
1	0	This combination addresses the <b>Offset Register</b> . One register in total.
1	1	This combination addresses the <b>Gain Register</b> . One register in total.

### Writing to/Reading from the Calibration Registers

For writing to the calibration registers a write to the control register is required to set the CALSLT0 and CALSLT1 bits. For reading from the calibration registers a write to the control register is required to set the CALSLT0 and CALSLT1 bits, but also to set the RDSLT1 and RDSLT0 bits to 10 (this addresses the calibration registers for reading). The calibration register pointer is reset on writing to the control register setting the CALSLT1 and CALSLT0 bits, or upon completion of all the calibration register write/read operations. When reset it points to the first calibration register in the selected write/read sequence. The calibration register pointer will point to the gain calibration register upon reset in all but one case, this case being where the offset calibration register is selected on its own (CALSLT1 = 1, CALSLT0 = 0). Where more than one calibration register is being accessed, the calibration register pointer will be automatically incremented after each calibration register write/read operation. The order in which the 10 calibration registers are arranged is shown in Figure 7. The user may abort at any time before all the calibration register write/read operations are completed, and the next control register write operation will reset the calibration register pointer. The flowchart in Figure 8 shows the sequence for writing to the calibration registers and Figure 9 for reading.

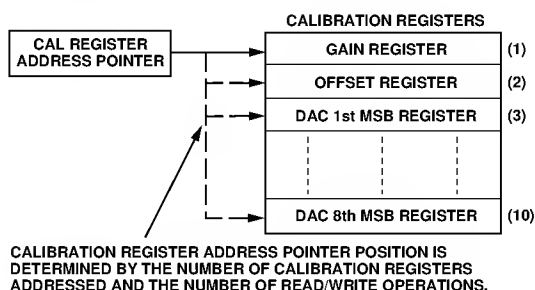


Figure 7. Calibration Register Arrangement

When reading from the calibration registers there will always be two leading zeros for each of the registers. When operating in serial Interface Mode 1, the read operations to the calibration registers cannot be aborted. The full number of read operations must be completed (see section on serial Interface Mode 1 timing for more detail).

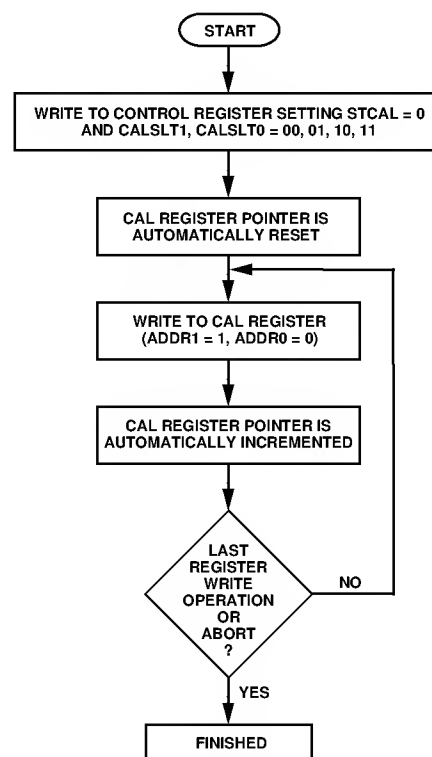


Figure 8. Flowchart for Writing to the Calibration Registers

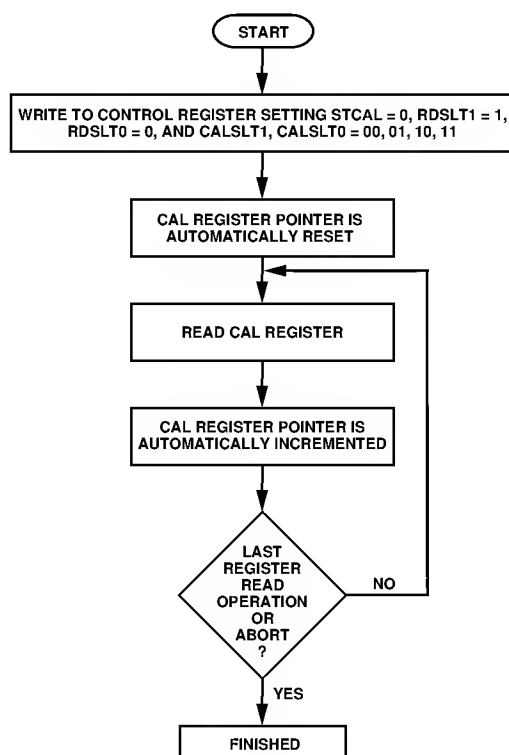


Figure 9. Flowchart for Reading from the Calibration Registers

#### Adjusting the Offset Calibration Register

The offset calibration register contains 16 bits, two leading zeros and 14 data bits. By changing the contents of the offset register, different amounts of offset on the analog input signal can be compensated for. Increasing the number in the offset calibration register compensates for negative offset on the analog input signal, and decreasing the number in the offset calibration register compensates for positive offset on the analog input signal. The default value of the offset calibration register is 0010 0000 0000 0000 approximately. This is not an exact value, but the value in the offset register should be close to this value. Each of the 14 data bits in the offset register is binary weighted; the MSB has a weighting of 5% of the reference voltage, the MSB-1 has a weighting of 2.5%, the MSB-2 has a weighting of 1.25%, and so on down to the LSB which has a weighting of 0.0006%.

This gives a resolution of  $\pm 0.0006\%$  of  $V_{REF}$  approximately. More accurately the resolution is  $\pm (0.05 \times V_{REF})/2^{13}$  volts =  $\pm 0.015$  mV, with a 2.5 V reference. The maximum offset that can be compensated for is  $\pm 5\%$  of the reference voltage, which equates to  $\pm 125$  mV with a 2.5 V reference and  $\pm 250$  mV with a 5 V reference.

*Q. If a +20 mV offset is present in the analog input signal and the reference voltage is 2.5 V, what code needs to be written to the offset register to compensate for the offset ?*

*A. 2.5 V reference implies that the resolution in the offset register is  $5\% \times 2.5 \text{ V}/2^{13} = 0.015$  mV.  $+20 \text{ mV}/0.015 \text{ mV} = 1310.72$ ; rounding to the nearest number gives 1311. In binary terms this is 0101 0001 1111, therefore decrease the offset register by 0101 0001 1111.*

This method of compensating for offset in the analog input signal allows for fine tuning the offset compensation. If the offset on the analog input signal is known, there will be no need to apply the offset voltage to the analog input pins and do a system calibration. The offset compensation can take place in software.

#### Adjusting the Gain Calibration Register

The gain calibration register contains 16 bits, two leading 0s and 14 data bits. The data bits are binary weighted as in the offset calibration register. The gain register value is effectively multiplied by the analog input to scale the conversion result over the full range. Increasing the gain register compensates for a smaller analog input range and decreasing the gain register compensates for a larger input range. The maximum analog input range that the gain register can compensate for is 1.025 times the reference voltage, and the minimum input range is 0.975 times the reference voltage.

# AD7853/AD7853L

## CIRCUIT INFORMATION

The AD7853/AD7853L is a fast, 12-bit single supply A/D converter. The part requires an external 4 MHz/1.8 MHz master clock (CLKIN), two  $C_{REF}$  capacitors, a  $\overline{CONVST}$  signal to start conversion and power supply decoupling capacitors. The part provides the user with track/hold, on-chip reference, calibration features, A/D converter and serial interface logic functions on a single chip. The A/D converter section of the AD7853/AD7853L consists of a conventional successive-approximation converter based around a capacitor DAC. The AD7853/AD7853L accepts an analog input range of 0 to  $+V_{DD}$  where the reference can be tied to  $V_{DD}$ . The reference input to the part is buffered on-chip.

A major advantage of the AD7853/AD7853L is that a conversion can be initiated in software as well as applying a signal to the  $\overline{CONVST}$  pin. Another innovative feature of the AD7853/AD7853L is self-calibration on power-up, which is initiated having a 0.01  $\mu F$  capacitor from the  $\overline{CAL}$  pin to AGND, to give superior dc accuracy. The part should be allowed 150 ms after power-up to perform this automatic calibration before any reading or writing takes place. The part is available in a 24-pin SSOP package and this offers the user considerable spacing saving advantages over alternative solutions. The AD7853L version typically consumes only 5.5 mW making it ideal for battery-powered applications.

## CONVERTER DETAILS

The master clock for the part must be applied to the CLKIN pin. Conversion is initiated on the AD7853/AD7853L by pulsing the  $\overline{CONVST}$  input or by writing to the control register and setting the  $\overline{CONVST}$  bit to 1. On the rising edge of  $\overline{CONVST}$  (or at the end of the control register write operation), the on-

chip track/hold goes from track to hold mode. The falling edge of the CLKIN signal which follows the rising edge of the edge of  $\overline{CONVST}$  signal initiates the conversion, provided the rising edge of  $\overline{CONVST}$  occurs at least 10 ns typically before this CLKIN edge. The conversion cycle will take 16.5 CLKIN periods from this CLKIN falling edge. If the 10 ns setup time is not met, the conversion will take 17.5 CLKIN periods. The maximum specified conversion time is 4.6  $\mu s$  for the AD7853 (18  $t_{CLKIN}$ , CLKIN = 4 MHz) and 10  $\mu s$  for the AD7853L (18  $t_{CLKIN}$ , CLKIN = 1.8 MHz). When a conversion is completed, the BUSY output goes low, and then the result of the conversion can be read by accessing the data through the serial interface. To obtain optimum performance from the part, the read operation should not occur during the conversion or 400 ns prior to the next  $\overline{CONVST}$  rising edge. However, the maximum throughput rates are achieved by reading/writing during conversion, and reading/writing during conversion is likely to degrade the Signal to (Noise + Distortion) by only 0.5 dBs. The AD7853 can operate at throughput rates up to 200 kHz, 100 kHz for the AD7853L. For the AD7853/AD7853L a conversion takes 18 CLKIN periods, 2 CLKIN periods are needed for the acquisition time giving a full cycle time of 5  $\mu s$  (= 200 kHz, CLKIN = 4 MHz). For the AD7853L 100 kHz throughput can be obtained as follows: the CLKIN and  $\overline{CONVST}$  signals are arranged to give a conversion time of 16.5 CLKIN periods as described above, 1.5 CLKIN periods are allowed for the acquisition time. This gives a full cycle time of 10  $\mu s$  (= 100 kHz, CLKIN = 1.8 MHz). When using the software conversion start for maximum throughput, the user must ensure the control register write operation extends beyond the falling edge of BUSY. The falling edge of BUSY resets the  $\overline{CONVST}$  bit to 0 and allows it to be reprogrammed to 1 to start the next conversion.

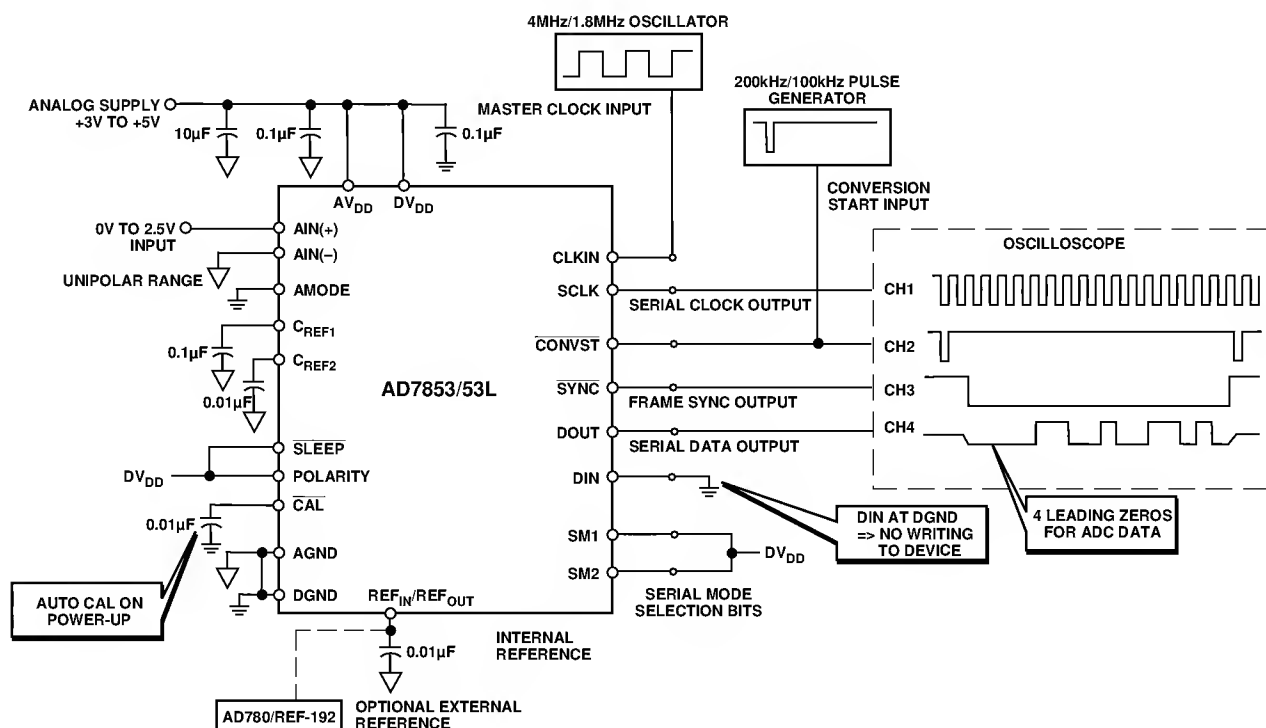


Figure 10. Typical Circuit

### TYPICAL CONNECTION DIAGRAM

Figure 10 shows a typical connection diagram for the AD7853/AD7853L. The DIN line is tied to DGND so that no data is written to the part. The AGND and the DGND pins are connected together at the device for good noise suppression. The CAL pin has a 0.01  $\mu\text{F}$  capacitor to enable an automatic self-calibration on power-up. The SCLK and SYNC are configured as outputs by having SM1 and SM2 at  $\text{DV}_{\text{DD}}$ . The conversion result is output in a 16-bit word with 4 leading zeros followed by the MSB of the 12-bit result. Note that after the  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  power-up, the part will require 150 ms for the internal reference to settle and for the automatic calibration on power-up to be completed.

For applications where power consumption is a major concern, the SLEEP pin can be connected to DGND. See Power-Down section for more detail on low power applications.

### ANALOG INPUT

The equivalent circuit of the analog input section is shown in Figure 11. During the acquisition interval the switches are both in the track position and the AIN(+) charges the 20 pF capacitor through the 125  $\Omega$  resistance. On the rising edge of CONVST $\bar$  switches SW1 and SW2 go into the hold position retaining charge on the 20 pF capacitor as a sample of the signal on AIN(+). The AIN(−) is connected to the 20 pF capacitor, and this unbalances the voltage at node A at the input of the comparator. The capacitor DAC adjusts during the remainder of the conversion cycle to restore the voltage at node A to the correct value. This action transfers a charge, representing the analog input signal, to the capacitor DAC which in turn forms a digital representation of the analog input signal. The voltage on the AIN(−) pin directly influences the charge transferred to the capacitor DAC at the hold instant. If this voltage changes during the conversion period, the DAC representation of the analog input voltage will be altered. Therefore it is most important that the voltage on the AIN(−) pin remains constant during the conversion period. Furthermore, it is recommended that the AIN(−) pin is always connected to AGND or to a fixed dc voltage.

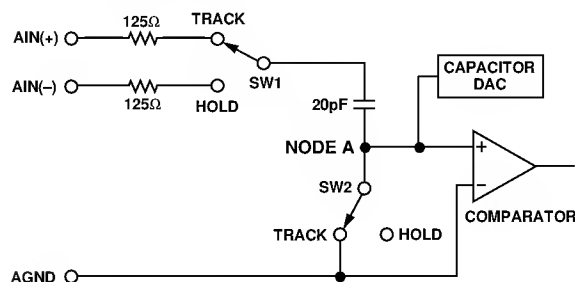


Figure 11. Analog Input Equivalent Circuit

### Acquisition Time

The track and hold amplifier enters its tracking mode on the falling edge of the BUSY signal. The time required for the track and hold amplifier to acquire an input signal will depend on how quickly the 20 pF input capacitance is charged. The acquisition time is calculated using the formula:

$$t_{ACQ} = 9 \times (R_{IN} + 125 \Omega) \times 20 \text{ pF}$$

where  $R_{IN}$  is the source impedance of the input signal, and 125  $\Omega$ , 20 pF is the input  $R$ ,  $C$ .

### DC/AC Applications

For dc applications high source impedances are acceptable, provided there is enough acquisition time between conversions to charge the 20 pF capacitor. The acquisition time can be calculated from the above formula for different source impedances. For example with  $R_{IN} = 5 \text{ k}\Omega$ , the required acquisition time will be 922 ns.

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the AIN(+) pin, as shown in Figure 13. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 12 shows a graph of the Total Harmonic Distortion vs. analog input signal frequency for different source impedances. With the setup as in Figure 13, the THD is at the −90 dB level. With a source impedance of 1 k $\Omega$  and no capacitor on the AIN(+) pin, the THD increases with frequency.

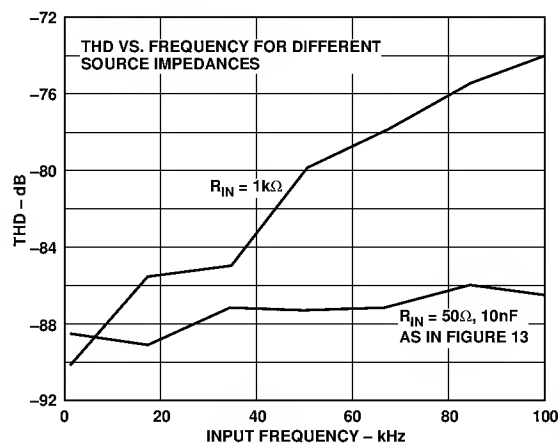


Figure 12. THD vs. Analog Input Frequency

In a single supply application (both 3 V and 5 V), the V+ and V− of the op amp can be taken directly from the supplies to the AD7853/AD7853L which eliminates the need for extra external power supplies. When operating with rail-to-rail inputs and outputs at frequencies greater than 10 kHz, care must be taken in selecting the particular op amp for the application. In particular, for single supply applications the input amplifiers should be connected in a gain of −1 arrangement to get the optimum performance. Figure 13 shows the arrangement for a single supply application with a 50  $\Omega$  and 10 nF low-pass filter (cutoff frequency 320 kHz) on the AIN(+) pin. Note that the 10 nF is a capacitor with good linearity to ensure good ac performance. Recommended single supply op amps are the AD820 and the AD820-3V.

# AD7853/AD7853L

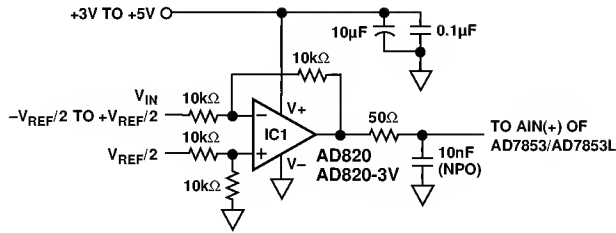


Figure 13. Analog Input Buffering

## Input Ranges

The analog input range for the AD7853/AD7853L is 0 V to  $V_{REF}$  in both the unipolar and bipolar ranges.

The only difference between the unipolar range and the bipolar range is that in the bipolar range the AIN(-) has to be biased up to  $+V_{REF}/2$  and the output coding is 2s complement (See Table V and Figures 14 and 15). The unipolar or bipolar mode is selected by the AMODE pin (0 for the unipolar range and 1 for the bipolar range).

Table V. Analog Input Connections

Analog Input Range	Input Connections	Connection Diagram	AMODE
0 V to $V_{REF}$ <sup>1</sup>	$V_{IN}$ AGND	Figure 14	DGND
$\pm V_{REF}/2$ <sup>2</sup>	$V_{IN}$ $V_{REF}/2$	Figure 15	DV <sub>DD</sub>

## NOTES

<sup>1</sup>Output code format is straight binary.

<sup>2</sup>Range is  $\pm V_{REF}/2$  biased about  $V_{REF}/2$ . Output code format is 2s complement.

Note that the AIN(-) pin on the AD7853/AD7853L can be biased up above AGND in the unipolar mode also, if required. The advantage of biasing the lower end of the analog input range away from AGND is that the user does not have to have the analog input swing all the way down to AGND. This has the advantage in true single supply applications that the input amplifier does not have to swing all the way down to AGND. The upper end of the analog input range is shifted up by the same amount. Care must be taken so that the bias applied does not shift the upper end of the analog input above the  $AV_{DD}$  supply. In the case where the reference is the supply,  $AV_{DD}$ , the AIN(-) must be tied to AGND in unipolar mode.

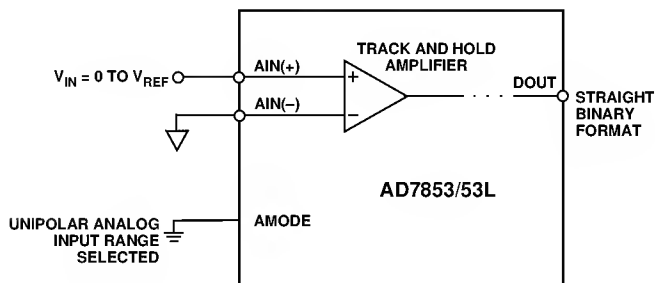


Figure 14. 0 to  $V_{REF}$  Unipolar Input Configuration

## Transfer Functions

For the unipolar range the designed code transitions occur midway between successive integer LSB values (i.e.,  $1/2$  LSB,  $3/2$  LSBs,  $5/2$  LSBs . . .  $FS - 3/2$  LSBs). The output coding is straight binary for the unipolar range with  $1 \text{ LSB} = FS/4096 =$

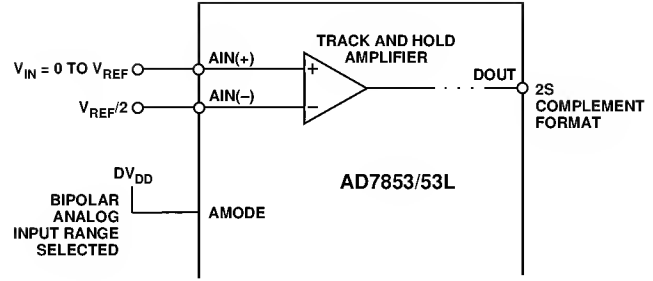


Figure 15.  $\pm V_{REF}/2$  about  $V_{REF}/2$  Bipolar Input Configuration

$3.3 \text{ V}/4096 = 0.8 \text{ mV}$  when  $V_{REF} = 3.3 \text{ V}$ . The ideal input/output transfer characteristic for the unipolar range is shown in Figure 16.

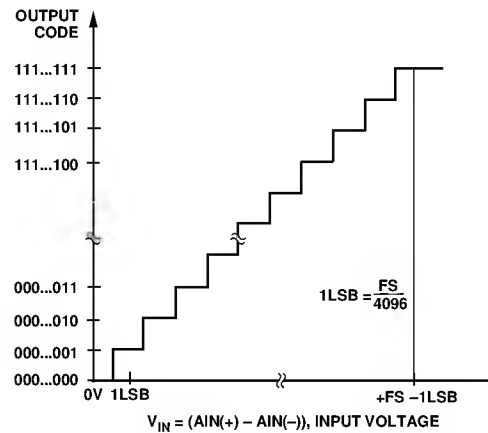


Figure 16. AD7853/AD7853L Unipolar Transfer Characteristic

Figure 15 shows the AD7853/AD7853L's  $\pm V_{REF}/2$  bipolar analog input configuration (where AIN(+) cannot go below 0 V so for the full bipolar range then the AIN(-) pin should be biased to  $+V_{REF}/2$ ). Once again the designed code transitions occur midway between successive integer LSB values. The output coding is 2s complement with  $1 \text{ LSB} = 4096 = 3.3 \text{ V}/4096 = 0.8 \text{ mV}$ . The ideal input/output transfer characteristic is shown in Figure 17.

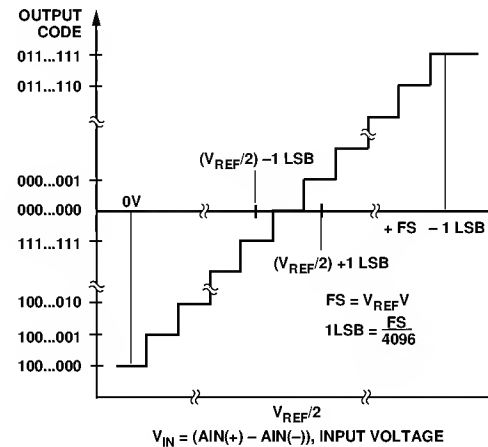


Figure 17. AD7853/AD7853L Bipolar Transfer Characteristic



## REFERENCE SECTION

For specified performance, it is recommended that when using an external reference this reference should be between 2.3 V and the analog supply  $AV_{DD}$ . The connections for the relevant reference pins are shown in the typical connection diagrams. If the internal reference is being used, the  $REF_{IN}/REF_{OUT}$  pin should have a 10 nF capacitor connected to AGND very close to the  $REF_{IN}/REF_{OUT}$  pin. These connections are shown in Figure 18.

If the internal reference is required for use external to the ADC, it should be buffered at the  $REF_{IN}/REF_{OUT}$  pin and a 10 nF capacitor connected from this pin to AGND. The typical noise performance for the internal reference, with 5 V supplies is 150 nV/ $\sqrt{\text{Hz}}$  @ 1 kHz and dc noise is 100  $\mu\text{V}$  p-p.

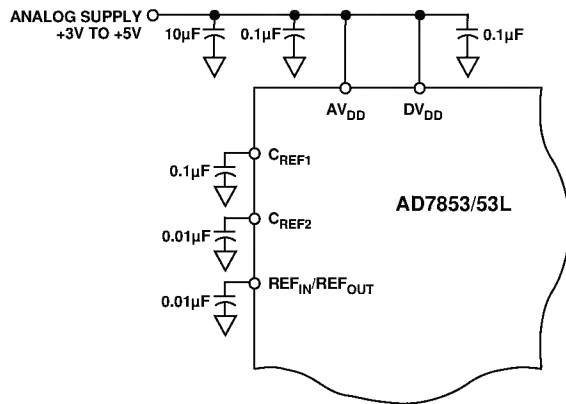


Figure 18. Relevant Connections When Using Internal Reference

The other option is that the  $REF_{IN}/REF_{OUT}$  pin be overdriven by connecting it to an external reference. This is possible due to the series resistance from the  $REF_{IN}/REF_{OUT}$  pin to the internal reference. This external reference can have a range that includes  $AV_{DD}$ . When using  $AV_{DD}$  as the reference source, the 10 nF capacitor from the  $REF_{IN}/REF_{OUT}$  pin to AGND should be as close as possible to the  $REF_{IN}/REF_{OUT}$  pin, and also the  $C_{REF1}$  pin should be connected to  $AV_{DD}$  to keep this pin at the same level as the reference. The connections for this arrangement are shown in Figure 19. When using  $AV_{DD}$  it may be necessary to add a resistor in series with the  $AV_{DD}$  supply. This will have the effect of filtering the noise associated with the  $AV_{DD}$  supply.

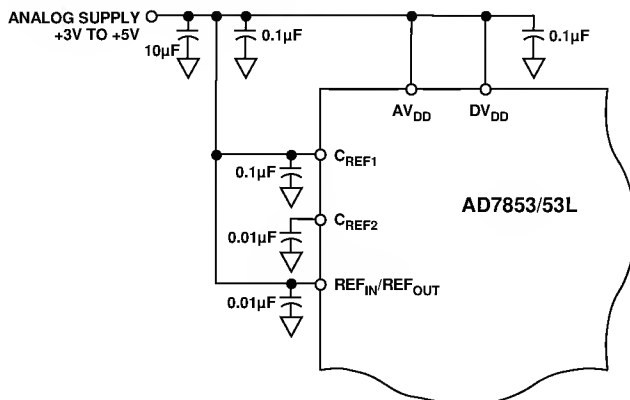


Figure 19. Relevant Connections When Using  $AV_{DD}$  as the Reference

## AD7853/AD7853L PERFORMANCE CURVES

Figure 20 shows a typical FFT plot for the AD7853 at 200 kHz sample rate and 10 kHz input frequency.

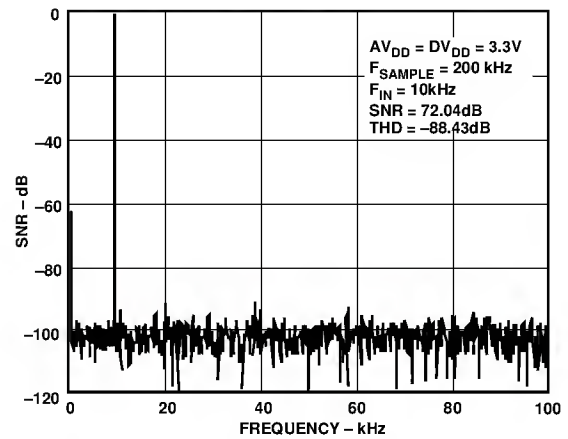


Figure 20. FFT Plot

Figure 21 shows the SNR versus Frequency for different supplies and different external references.

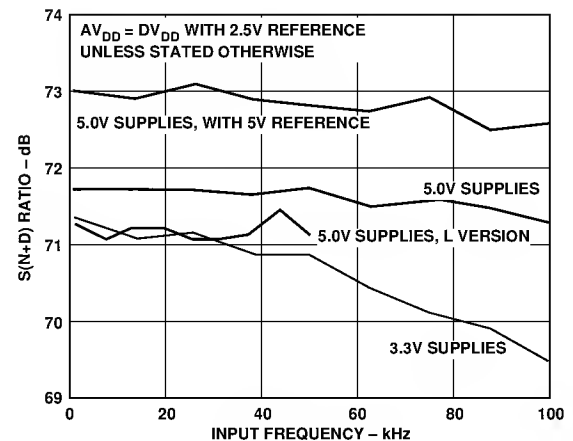


Figure 21. SNR vs. Frequency

Figure 22 shows the Power Supply Rejection Ratio versus Frequency for the part. The Power Supply Rejection Ratio is defined as the ratio of the power in ADC output at frequency  $f$  to the power of a full-scale sine wave.

$$PSRR \text{ (dB)} = 10 \log (P_f/P_{fs})$$

$P_f$  = Power at frequency  $f$  in ADC output,  $P_{fs}$  = power of a full-scale sine wave. Here a 100 mV peak-to-peak sine wave is coupled onto the  $AV_{DD}$  supply while the digital supply is left unaltered. Both the 3.3 V and 5.0 V supply performances are shown.

# AD7853/AD7853L

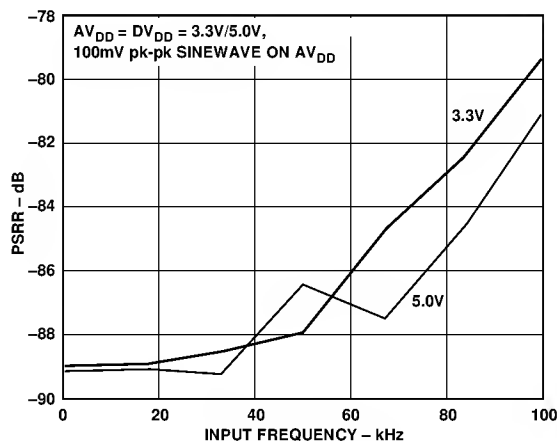


Figure 22. PSRR vs. Frequency

## POWER-DOWN OPTIONS

The AD7853/AD7853L should be left idle for 150 ms typically after the  $AV_{DD}$  and the  $DV_{DD}$  power-up to allow for the internal reference to settle and the automatic calibration on power-up to be completed. The  $SLEEP$  pin can be hardwired to  $DGND$  before power-up as the part will disable the function of the  $SLEEP$  pin while the automatic calibration on power-up is being performed.

The AD7853/AD7853L provides a number of power-down options. The two modes are the Full Power-Down and the Partial Power-Down. These options are controlled by the  $PMGT1$  and  $PMGT0$  bits in the control register. When both these bits are 0

(default status on power-up), the  $SLEEP$  pin determines whether the AD7853/AD7853L is in normal mode of operation or whether it enters full power-down mode after every conversion. With these bits at 0, 1 the AD7853/AD7853L operates in normal mode regardless of the status of the  $SLEEP$ . With these bits at 1, 0 the part enters a full power-down mode, again independent of the  $SLEEP$  pin. Finally, with these bits at 1, 1 the part enters its partial power-down. The advantage of the partial power-down is that the part will require significantly less time to “power-up” than from the full power-down. In this partial power-down, the reference voltage stays powered up so if this is being used external to the AD7853/AD7853L it is still available even though the AD7853/AD7853L is effectively powered down. Table VI summarizes the power management options while Table VII shows typical power-up times when using the 2.5 V internal reference. The capacitor values between  $C_{REF1}$ ,  $C_{REF2}$ ,  $REF_{IN}/REF_{OUT}$  and  $AGND$  are also listed. The power-up time is defined as the time taken for the output code to settle to within  $\pm 0.5$  LSBs of its final value. If a power-up time shorter than that quoted in Table VII is used, the error associated with the output code will increase. For a power-up time of 10  $\mu s$  from partial power-down mode, the output code will be settled to within  $\pm 3$  LSBs typically of its final value. When using  $AV_{DD}$  as the reference, the power-up time required will be less than the figures quoted in Table VII.

A typical connection diagram for a low power application is shown in Figure 23 (AD7853L is the low power version of the AD7853).

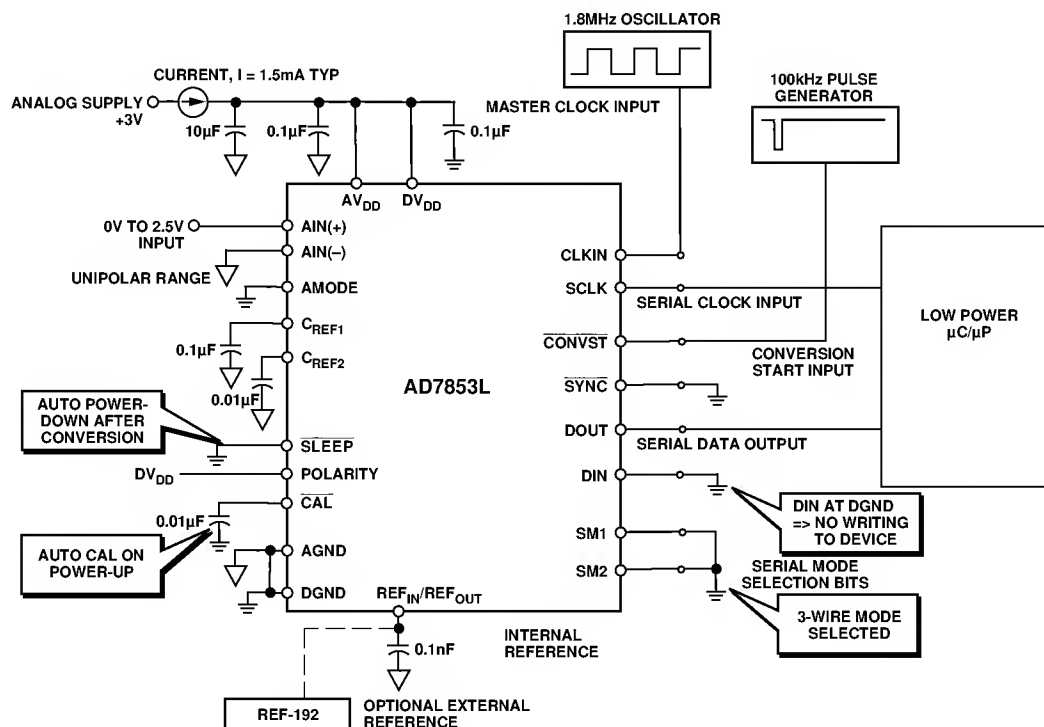


Figure 23. Typical Low Power Circuit

Table VI. Power Management Options

PMGT1 Bit	PMGT0 Bit	SLEEP Pin	Comment
0	0	0	<b>Full Power-Down</b> if Not Calibrating or Converting (Default Condition After Power-On)
0	0	1	<b>Normal Operation</b>
0	1	X	<b>Normal Operation</b> (Independent of the $\overline{\text{SLEEP}}$ Pin)
1	0	X	<b>Full Power-Down</b>
1	1	X	<b>Partial Power-Down</b> if Not Converting

Table VII. Power-Up Times

$C_{\text{REF1}}$ (nF)	$C_{\text{REF2}}$ (nF)	Reference Capacitor (nF)	Power-Down Mode	Power-Up Delay ( $\mu\text{s}$ )
100	10	0.1	Full	300
100	10	0.1	Partial	50
10	1	0.1	Full	300
10	1	0.1	Partial	50

**POWER-UP/DOWN SEQUENCE**

Power-up times and throughput rates quoted in this section are based on using the 2.5 V internal reference. If an external reference is used and is powered on constantly, or if  $\text{AV}_{\text{DD}}$  is used as the reference, then the power-up times will be shorter and the throughput rates higher.

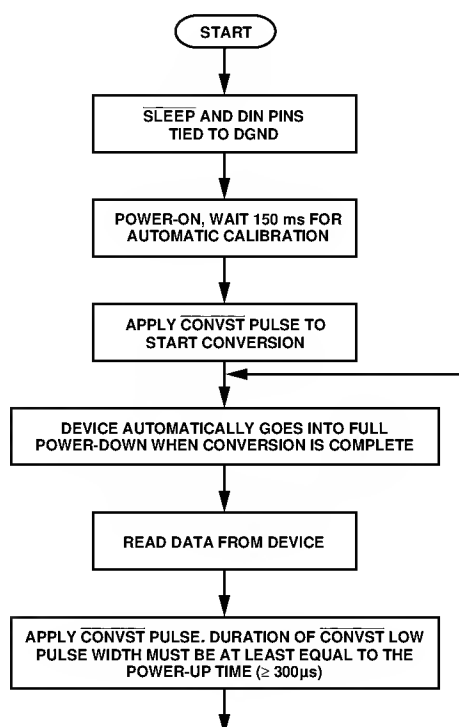


Figure 24. Flowchart for Typical Power Down/Up Sequence with No Writing to AD7853/AD7853L

**No Writing to AD7853/AD7853L (DIN LOW)**

If the DIN is hardwired to DGND (so that there is no writing to the part), the PMGT1 and PMGT0 bits in the Control Register are at their default value of 0, 0. The  $\overline{\text{SLEEP}}$  pin will then determine whether the part is in power-down or not. Tying the  $\overline{\text{SLEEP}}$  pin to DGND will cause the device to go into full power-down when there is no conversion or calibration taking place. In this case the  $\overline{\text{CONVST}}$  falling edge will “wake-up” the part. The  $\overline{\text{CONVST}}$  must remain low for at least the power-up time quoted in Table III as shown in Figure 25. This will allow the part to be settled before the start of the next conversion. The maximum throughput rate in this case will be limited to 2 kHz.

Figure 24 shows a typical power-up/down sequence with no writing to the AD7853/AD7853L.

**Writing to AD7853/AD7853L**

The sequence of events here use the CONVST bit in the control register to start the conversion. Alternatively the  $\overline{\text{CONVST}}$  pin may be used as in Figure 25. When writing to the AD7853/AD7853L there are a number of different ways in utilizing the power-down options. For applications which require throughput rates of less than 2 kHz, a full/partial power-down mode combination, or a full power-down mode on its own, may be used. For higher throughput rates the partial power-down mode should be used. Table VIII shows the recommended power-down mode for lowest current at a given throughput rate.

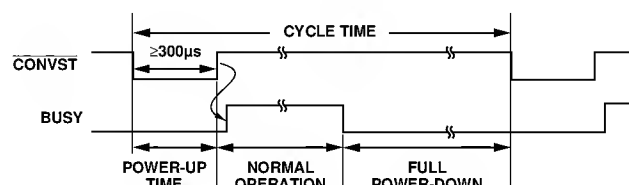


Figure 25. Timing for Flowchart Sequence of Figure 24

Table VIII. Recommended Power-Down Mode for Lowest  $I_{\text{DD}}$ 

Power-Down Mode	Maximum Throughput Rate
Full/Partial Combination	2 kHz
Partial	16 kHz

**Using Full and Partial Power-Down Combination**

Using a full/partial power-down mode combination has the benefits of the low current associated with a full power-down and the speed of powering up from a partial power-down. It will also give the lowest current for a given throughput rate, one third of the current when using the full power-down mode on its own. Figures 26 and 27 show the recommended sequence and the relevant timing signals. For the all 0s write operation described in the sequence, only the two MSBs need to be 0 to ensure that the rest of the data write is ignored, but it is just as easy to write all 0s. The Supply Current versus Throughput rate for this power up/power down sequence is shown in Figure 28.

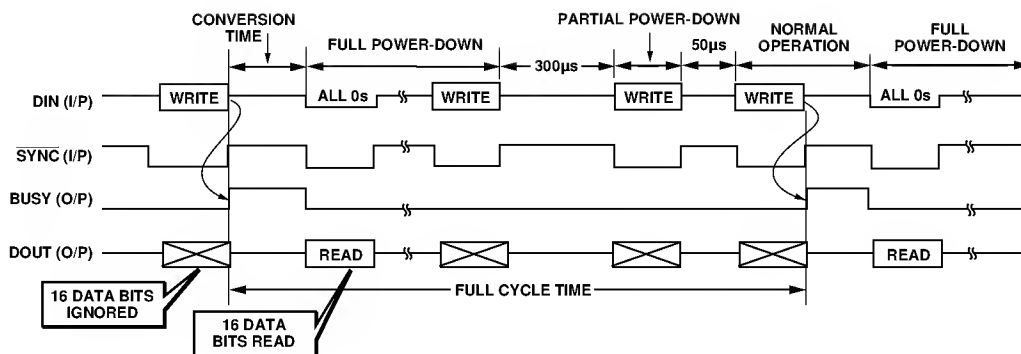


Figure 26. Timing Sequence for Full/Partial Power-Down Combination

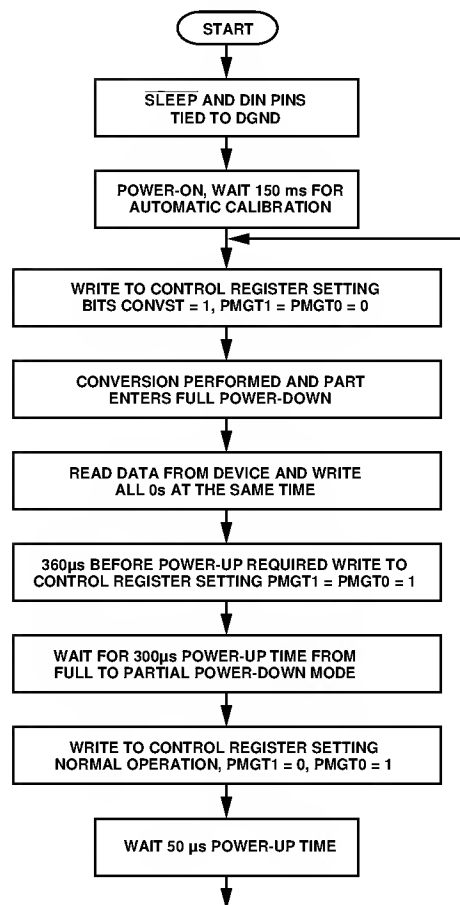


Figure 27. Flowchart for Full/Partial Power-Down Mode Combination

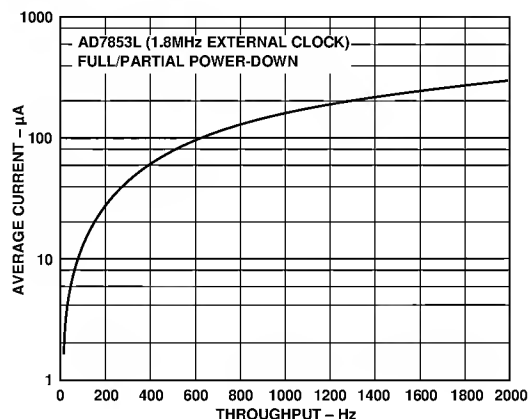


Figure 28. Supply Current vs. Throughput Rate with Full/Partial Power-Down Combination (Sequence as Illustrated in Figures 26 and 27)

#### Full Power-Down or Partial Power-Down

In some applications it may not be feasible to use a combination of full and partial power-down as shown in Figures 26 and 27. This may be for software overhead reasons or for applications requiring throughput rates greater than 2 kHz.

Using full power-down only allows for a maximum throughput rate of 2 kHz, but the supply current will be three times or greater than for the full/partial power-down combination sequence described in Figures 26 and 27.

Using partial power-down allows for throughput rates up to 16 kHz (if  $AV_{DD}$  is used as the reference, the throughput rates will be > 16 kHz). Figures 29 and 30 show the timing/flowchart for power-up/down when using the partial power-down mode only. Figure 31 shows the Supply Current vs. Throughput rate for this sequence.

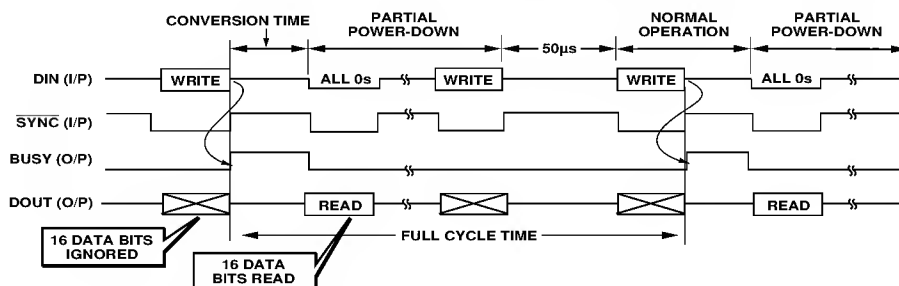


Figure 29. Timing Sequence for Partial Power-Down Only

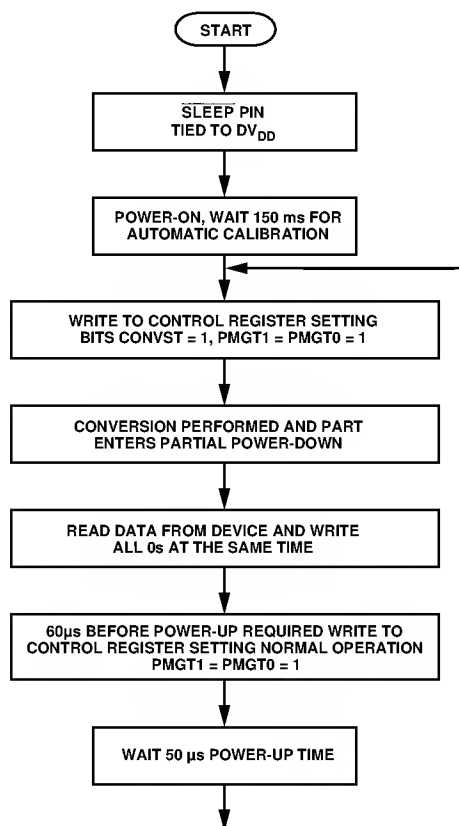


Figure 30. Flowchart for Partial Power-Down Only

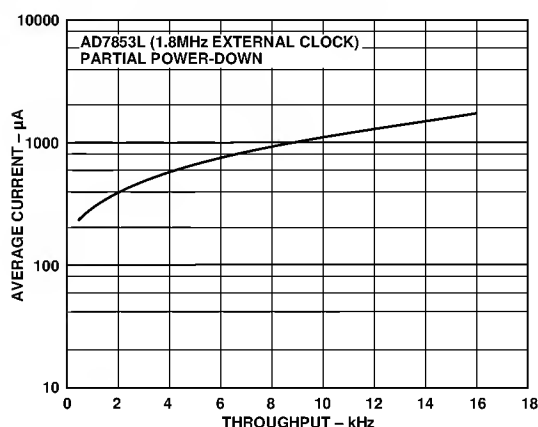


Figure 31. Supply Current vs. Throughput Rate with Partial Power-Down Only (Sequence as Illustrated in Figures 29 and 30)

**NOTE**

When setting the power-down mode by writing to the part, it is recommended to be operating in an interface mode other than Interface Modes 4, and 5. This way the user has more control to initiate power-down, and power-up commands.

**CALIBRATION SECTION****Calibration Overview**

The automatic calibration that is performed on power-up ensures that the calibration options covered in this section will not be required in a significant amount of applications. The user will not have to initiate a calibration unless the operating conditions change (CLKIN frequency, analog input mode, reference voltage, temperature, and supply voltages). The AD7853/AD7853L have a number of calibration features that may be required in some applications and there are a number of advantages in performing these different types of calibration. First, the internal errors in the ADC can be reduced significantly to give superior dc performance; and second, system offset and gain errors can be removed. This allows the user to remove reference errors (whether it be internal or external reference) and to make use of the full dynamic range of the AD7853/AD7853L by adjusting the analog input range of the part for a specific system.

There are two main calibration modes on the AD7853/AD7853L, self-calibration and system calibration. There are various options in both self-calibration and system calibration as outlined previously in Table III. All the calibration functions can be initiated by pulsing the  $\overline{\text{CAL}}$  pin or by writing to the control register and setting the STCAL bit to 1. The timing diagrams that follow involve using the  $\overline{\text{CAL}}$  pin.

The duration of each of the different types of calibrations is given in Table IX for the AD7853 with a 4 MHz master clock. These calibration times are master clock dependent. Therefore the calibration times for the AD7853L (CLKIN = 1.8 MHz) will be larger than those quoted in Table IX.

**Table IX. Calibration Times (AD7853 with 4 MHz CLKIN)**

Type of Self- or System Calibration	Time
Full	31.25 ms
Gain + Offset	6.94 ms
Offset	3.47 ms
Gain	3.47 ms

**Automatic Calibration on Power-On**

The  $\overline{\text{CAL}}$  pin has a 0.15  $\mu\text{A}$  pull-up current source connected to it internally to allow for an automatic full self-calibration on power-on. A full self-calibration will be initiated on power-on if a 10 nF capacitor is connected from the  $\overline{\text{CAL}}$  pin to AGND. The internal current source connected to the  $\overline{\text{CAL}}$  pin charges up the external capacitor and the time required to charge the external capacitor will be 100 ms approximately. This time is large enough to ensure that the internal reference is settled before the calibration is performed. However, if an external reference is being used, this reference must have stabilized before the automatic calibration is initiated (if larger time than 100 ms is required then a larger capacitor on the  $\overline{\text{CAL}}$  pin should be used). After this 100 ms has elapsed, the calibration will be performed which will take 32/72 ms (4 MHz / 1.8 MHz CLKIN). Therefore 132/172 ms should be allowed before operating the part. After calibration, the part is accurate to the 12-bit level and the specifications quoted on the data sheet apply. There will be no need to perform another calibration unless the operating conditions change or unless a system calibration is required.

# AD7853/AD7853L

## Self-Calibration Description

There are a four different calibration options within the self-calibration mode. There is a full self-calibration where the DAC, internal offset, and internal gain errors are calibrated out. Then, there is the (Gain + Offset) self-calibration which calibrates out the internal gain error and then the internal offset errors. The internal DAC is not calibrated here. Finally, there are the self-offset and self-gain calibrations which calibrate out the internal offset errors and the internal gain errors respectively.

The internal capacitor DAC is calibrated by trimming each of the capacitors in the DAC. It is the ratio of these capacitors to each other that is critical, and so the calibration algorithm ensures that this ratio is at a specific value by the end of the calibration routine. For the offset and gain there are two separate capacitors, one of which is trimmed when an offset or gain calibration is performed. Again it is the ratio of these capacitors to the capacitors in the DAC that is critical and the calibration algorithm ensures that this ratio is at a specified value for both the offset and gain calibrations.

In Bipolar Mode the midscale error is adjusted for an offset calibration and the positive full-scale error is adjusted for the gain calibration; in Unipolar Mode the zero-scale error is adjusted for an offset calibration and the positive full-scale error is adjusted for a gain calibration.

## Self-Calibration Timing

The diagram of Figure 32 shows the timing for a full self-calibration. Here the BUSY line stays high for the full length of the self-calibration. A self-calibration is initiated by bringing the CAL pin low (which initiates an internal reset) and then high again or by writing to the control register and setting the STCAL bit to 1 (note that if the part is in a power-down mode, the CAL pulse width must take account of the power-up time). The BUSY line is triggered high from the rising edge of CAL (or the end of the write to the control register if calibration is initiated in software), and BUSY will go low when the full self-calibration is complete after a time  $t_{CAL}$  as shown in Figure 32.

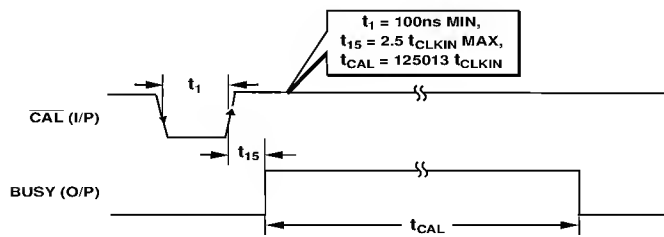


Figure 32. Timing Diagram for Full Self-Calibration

For the self-(gain + offset), self-offset and self-gain calibrations, the BUSY line will be triggered high by the rising edge of the CAL signal (or the end of the write to the control register if calibration is initiated in software) and will stay high for the full duration of the self-calibration. The length of time that the BUSY is high for will depend on the type of self-calibration that is initiated. Typical figures are given in Table IX. The timing diagrams for the other self-calibration options will be similar to that outlined in Figure 32.

## System Calibration Description

System calibration allows the user to take out system errors external to the AD7853/AD7853L as well as calibrate the errors of the AD7853/AD7853L itself. The maximum calibration range for the system offset errors is  $\pm 5\%$  of  $V_{REF}$  and for the system gain errors is  $\pm 2.5\%$  of  $V_{REF}$ . This means that the maximum allowable system offset voltage applied between the AIN(+) and AIN(-) pins for the calibration to adjust out this error is  $\pm 0.05 \times V_{REF}$  (i.e., the AIN(+) can be  $0.05 \times V_{REF}$  above AIN(-) or  $0.05 \times V_{REF}$  below AIN(-)). For the system gain error the maximum allowable system full-scale voltage, in unipolar mode, that can be applied between AIN(+) and AIN(-) for the calibration to adjust out this error is  $V_{REF} \pm 0.025 \times V_{REF}$  (i.e., the AIN(+) can be  $V_{REF} + 0.025 \times V_{REF}$  above AIN(-) or  $V_{REF} - 0.025 \times V_{REF}$  above AIN(-)). If the system offset or system gain errors are outside the ranges mentioned, the system calibration algorithm will reduce the errors as much as the trim range allows.

Figures 33 through 35 illustrate why a specific type of system calibration might be used. Figure 33 shows a system offset calibration (assuming a positive offset) where the analog input range has been shifted upwards by the system offset after the system offset calibration is completed. A negative offset may also be accounted for by a system offset calibration.

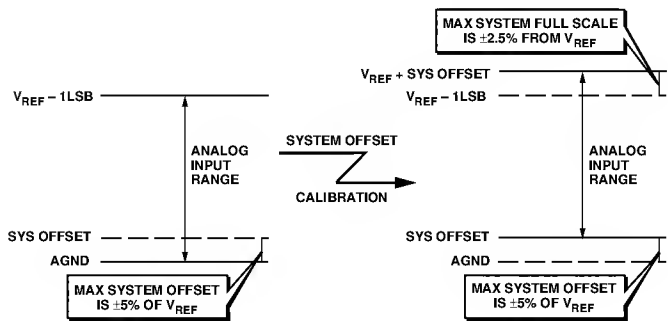


Figure 33. System Offset Calibration

Figure 34 shows a system gain calibration (assuming a system full scale greater than the reference voltage) where the analog input range has been increased after the system gain calibration is completed. A system full-scale voltage less than the reference voltage may also be accounted for by a system gain calibration.

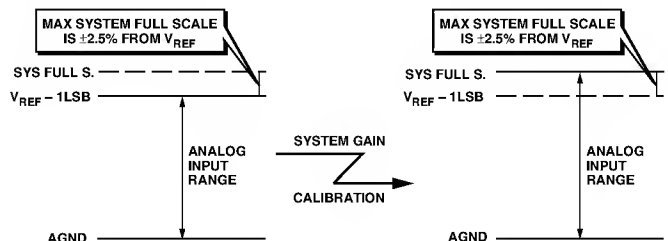


Figure 34. System Gain Calibration

Finally in Figure 35 both the system offset and gain are accounted for by the system offset followed by a system gain calibration. First the analog input range is shifted upwards by the positive system offset and then the analog input range is adjusted at the top end to account for the system full scale.

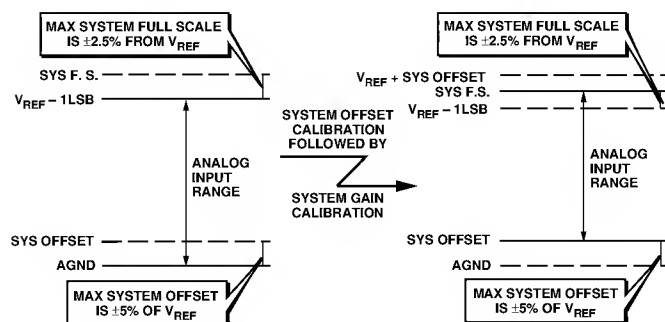


Figure 35. System (Gain + Offset) Calibration

#### System Gain and Offset Interaction

The inherent architecture of the AD7853/AD7853L leads to an interaction between the system offset and gain errors when a system calibration is performed. Therefore it is recommended to perform the cycle of a system offset calibration followed by a system gain calibration twice. Separate system offset and system gain calibrations reduce the offset and gain errors to at least the 12-bit level. By performing a system offset calibration first and a system gain calibration second, priority is given to reducing the gain error to zero before reducing the offset error to zero. If the system errors are small, a system offset calibration would be performed, followed by a system gain calibration. If the systems errors are large (close to the specified limits of the calibration range), this cycle would be repeated twice to ensure that the offset and gain errors were reduced to at least the 12-bit level. The advantage of doing separate system offset and system gain calibrations is that the user has more control over when the analog inputs need to be at the required levels, and the CONVST signal does not have to be used.

Alternatively, a system (gain + offset) calibration can be performed. It is recommended to perform three system (gain + offset) calibrations to reduce the offset and gain errors to the 12-bit level. For the system (gain + offset) calibration priority is given to reducing the offset error to zero before reducing the gain error to zero. Thus if the system errors are small then two system (gain + offset) calibrations will be sufficient. If the system errors are large (close to the specified limits of the calibration range), three system (gain + offset) calibrations may be required to reduce the offset and gain errors to at least the 12-bit level. There will never be any need to perform more than three system (offset + gain) calibrations.

In Bipolar Mode the midscale error is adjusted for an offset calibration and the positive full-scale error is adjusted for the gain calibration; in Unipolar Mode the zero-scale error is adjusted for an offset calibration and the positive full-scale error is adjusted for a gain calibration.

# AD7853/AD7853L

## System Calibration Timing

The calibration timing diagram in Figure 36 is for a full system calibration where the falling edge of  $\overline{\text{CAL}}$  initiates an internal reset before starting a calibration (note that if the part is in power-down mode the  $\overline{\text{CAL}}$  pulse width must take account of the power-up time). If a full system calibration is to be performed in software, it is easier to perform separate gain and offset calibrations so that the  $\text{CONVST}$  bit in the control register does not have to be programmed in the middle of the system calibration sequence. The rising edge of  $\overline{\text{CAL}}$  starts calibration of the internal DAC and causes the  $\text{BUSY}$  line to go high. If the control register is set for a full system calibration, the  $\text{CONVST}$  must be used also. The full-scale system voltage should be applied to the analog input pins from the start of calibration. The  $\text{BUSY}$  line will go low once the DAC and system gain calibration are complete. Next the system offset voltage is applied to the  $\text{AIN}$  pin for a minimum setup time ( $t_{\text{SETUP}}$ ) of 100 ns before the rising edge of the  $\text{CONVST}$  and remain until the  $\text{BUSY}$  signal goes low. The rising edge of the  $\text{CONVST}$  starts the system offset calibration section of the full system calibration and also causes the  $\text{BUSY}$  signal to go high. The  $\text{BUSY}$  signal will go low after a time  $t_{\text{CAL2}}$  when the calibration sequence is complete.

The timing for a system (gain + offset) calibration is very similar to that of Figure 36, the only difference being that the time  $t_{\text{CAL1}}$  will be replaced by a shorter time of the order of  $t_{\text{CAL2}}$  as the internal DAC will not be calibrated. The  $\text{BUSY}$  signal will signify when the gain calibration is finished and when the part is ready for the offset calibration.

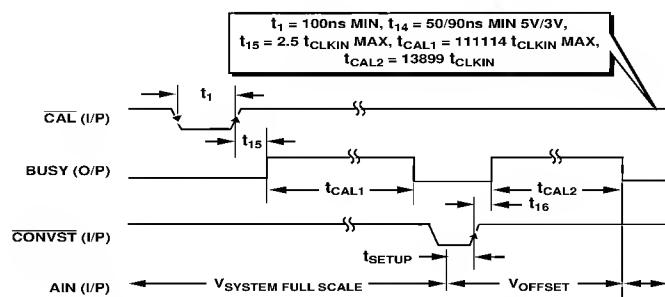


Figure 36. Timing Diagram for Full System Calibration

The timing diagram for a system offset or system gain calibration is shown in Figure 37. Here again the  $\overline{\text{CAL}}$  is pulsed and the rising edge of the  $\overline{\text{CAL}}$  initiates the calibration sequence (or the calibration can be initiated in software by writing to the control register). The rising edge of the  $\overline{\text{CAL}}$  causes the  $\text{BUSY}$  line to go high and it will stay high until the calibration sequence is finished. The analog input should be set at the correct level for a minimum setup time ( $t_{\text{SETUP}}$ ) of 100 ns before the rising edge of  $\overline{\text{CAL}}$  and stay at the correct level until the  $\text{BUSY}$  signal goes low.

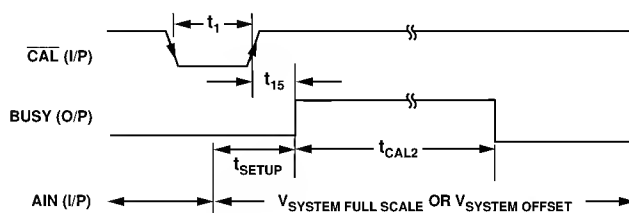


Figure 37. Timing Diagram for System Gain or System Offset Calibration



**SERIAL INTERFACE SUMMARY**

Table X details the five interface modes and the serial clock edges from which the data is clocked out by the AD7853/AD7853L (DOUT Edge) and that the data is latched in on (DIN Edge). The logic level of the POLARITY pin is shown and it is clear that this reverses the edges.

In Interface Modes 4 and 5 the  $\overline{\text{SYNC}}$  always clocks out the first data bit and SCLK will clock out the subsequent bits.

In Interface Modes 1, 2, and 3 the  $\overline{\text{SYNC}}$  is gated with the SCLK and the POLARITY pin. Thus the  $\overline{\text{SYNC}}$  may clock out the MSB of data. Subsequent bits will be clocked out by the serial clock, SCLK. The conditions for the  $\overline{\text{SYNC}}$  clocking out the MSB of data is as follows:

*With the POLARITY pin high the falling edge of  $\overline{\text{SYNC}}$  will clock out the MSB if the serial clock is low when the  $\overline{\text{SYNC}}$  goes low.*

*With the POLARITY pin low the falling edge of  $\overline{\text{SYNC}}$  will clock out the MSB if the serial clock is high when the  $\overline{\text{SYNC}}$  goes low.*

**Table X. SCLK Active Edge for Different Interface Modes**

Interface Mode	POLARITY Pin	DOUT Edge	DIN Edge
1, 2, 3	0 1	SCLK $\uparrow$ SCLK $\downarrow$	SCLK $\downarrow$ SCLK $\uparrow$
4, 5	0 1	SCLK $\downarrow$ SCLK $\uparrow$	SCLK $\uparrow$ SCLK $\downarrow$

**Resetting the Serial Interface**

When writing to the part via the DIN line there is the possibility of writing data into the incorrect registers, such as the test register for instance, or writing the incorrect data and corrupting the serial interface. The  $\overline{\text{SYNC}}$  pin acts as a reset. Bringing the  $\overline{\text{SYNC}}$  pin high resets the internal shift register. The first data bit after the next  $\overline{\text{SYNC}}$  falling edge will now be the first bit of a new 16-bit transfer. It is also possible that the test register contents were altered when the interface was lost. Therefore, once the serial interface is reset, it may be necessary to write the 16-bit word 0100 0000 0000 0000 to restore the test register to its default value. Now the part and serial interface are completely reset. It is always useful to retain the ability to program the  $\overline{\text{SYNC}}$  line from a port of the  $\mu$ Controller/DSP to have the ability to reset the serial interface.

Table XI summarizes the interface modes provided by the AD7853/AD7853L. It also outlines the various  $\mu$ P/ $\mu$ C to which the particular interface is suited.

The interface mode is determined by the serial mode selection pins SM1 and SM2. Interface mode 2 is the default mode. Note that Interface Mode 1 and 2 have the same combination of SM1 and SM2. Interface mode 1 may only be set by programming the control register (see section on control register). External SCLK and  $\overline{\text{SYNC}}$  signals ( $\overline{\text{SYNC}}$  may be hardwired low) are required for Interfaces Modes 1, 2, and 3. In Interface Modes 4 and 5 the AD7853/AD7853L generates the SCLK and  $\overline{\text{SYNC}}$ .

Some of the more popular  $\mu$ Processors,  $\mu$ Controllers, and the DSP machines that the AD7853/AD7853L will interface to directly are mentioned here. This does not cover all  $\mu$ Cs,  $\mu$ Ps and DSPs. The interface mode of the AD7853/AD7853L that is mentioned here for a specific  $\mu$ C,  $\mu$ P, or DSP is only a guide and in most cases another interface mode may work just as well.

A more detailed timing description on each of the interface modes follows.

**Table XI. Interface Mode Description**

SM1 Pin	SM2 Pin	$\mu$ Processor/ $\mu$ Controller	Interface Mode
0	0	8XC51 8XL51 PIC17C42	1 (2-Wire) (DIN is an Input/ Output pin)
0	0	68HC11 68L11	2 (3-Wire, SPI/QSPI) (Default Mode)
0	1	68HC16 PIC16C64 ADSP-21xx DSP56000 DSP56001 DSP56002 DSP56L002 TMS320C30	3 (QSPI) (External Serial Clock, SCLK, and External Frame Sync, $\overline{\text{SYNC}}$ , are required)
1	0	68HC16	4 (DSP is Slave) (AD7853/AD7853L generates a noncontinuous (16 clocks) Serial Clock, SCLK, and the Frame Sync, $\overline{\text{SYNC}}$ )
1	1	ADSP-21xx DSP56000 DSP56001 DSP56002 DSP56L002 TMS320C20 TMS320C25 TMS320C30 TMS320C5X TMS320LC5X	5 (DSP is Slave) (AD7853/AD7853L generates a continuous Serial Clock, SCLK, and the Frame Sync, $\overline{\text{SYNC}}$ )



**MODE 2 (3-Wire SPI/QSPI Interface Mode)****This is the DEFAULT INTERFACE MODE.**

In Figure 40 below we have the timing diagram for Interface Mode 2 which is the SPI/QSPI interface mode. Here the  $\overline{\text{SYNC}}$  input is active low and may be pulsed or tied permanently low. If  $\overline{\text{SYNC}}$  is permanently low 16 clock pulses must be applied to the SCLK pin for the part to operate correctly, and with a pulsed  $\overline{\text{SYNC}}$  input a continuous SCLK may be applied provided  $\overline{\text{SYNC}}$  is low for only 16 SCLK cycles. In Figure 30 the  $\overline{\text{SYNC}}$  going low disables the three-state on the DOUT pin. The first falling edge of the SCLK after the  $\overline{\text{SYNC}}$  going low clocks out the first leading zero on the DOUT pin. The DOUT pin is 3-stated again a time  $t_{12}$  after the  $\overline{\text{SYNC}}$  goes high. With the DIN pin the data input has to be set up a time  $t_7$  before the SCLK rising edge as the part samples the input data on the SCLK rising edge in this case. The POLARITY pin may be used to change the SCLK edge which the data is sampled on and clocked out on. If resetting the interface is required, the  $\overline{\text{SYNC}}$  must be taken high and then low.

**MODE 3 (QSPI Interface Mode)**

Figure 41 shows the timing diagram for Interface Mode 3. In this mode the DSP is the master and the part is the slave. Here the  $\overline{\text{SYNC}}$  input is edge triggered from high to low, and the 16 clock pulses are counted from this edge. Since the clock pulses

are counted internally then the  $\overline{\text{SYNC}}$  signal does not have to go high after the 16th SCLK rising edge as shown by the dotted  $\overline{\text{SYNC}}$  line in Figure 41. Thus a frame sync that gives a high pulse, of one SCLK cycle minimum duration, at the beginning of the read/write operation may be used. The rising edge of  $\overline{\text{SYNC}}$  enables the 3-state on the DOUT pin. The falling edge of  $\overline{\text{SYNC}}$  disables the 3-state on the DOUT pin, and data is clocked out on the falling edge of SCLK. Once  $\overline{\text{SYNC}}$  goes high, the 3-state on the DOUT pin is enabled. The data input is sampled on the rising edge of SCLK and thus has to be valid a time  $t_7$  before this rising edge. The POLARITY pin may be used to change the SCLK edge which the data is sampled on and clocked out on. If resetting the interface is required, the  $\overline{\text{SYNC}}$  must be taken high and then low.

**MODE 4 and 5 (Self-Clocking Modes)**

The timing diagrams in Figure 43 and Figure 44 are for Interface Modes 4 and 5. Interface Mode 4 has a noncontinuous SCLK output and Interface Mode 5 has a continuous SCLK output. These modes of operation are especially different to all the other modes since the SCLK and  $\overline{\text{SYNC}}$  are outputs. The  $\overline{\text{SYNC}}$  is generated by the part as is the SCLK. The master clock at the CLKIN pin is routed directly to the SCLK pin for Interface Mode 5 (Continuous SCLK) and the CLKIN signal is gated with the  $\overline{\text{SYNC}}$  to give the SCLK (noncontinuous) for Interface Mode 4.

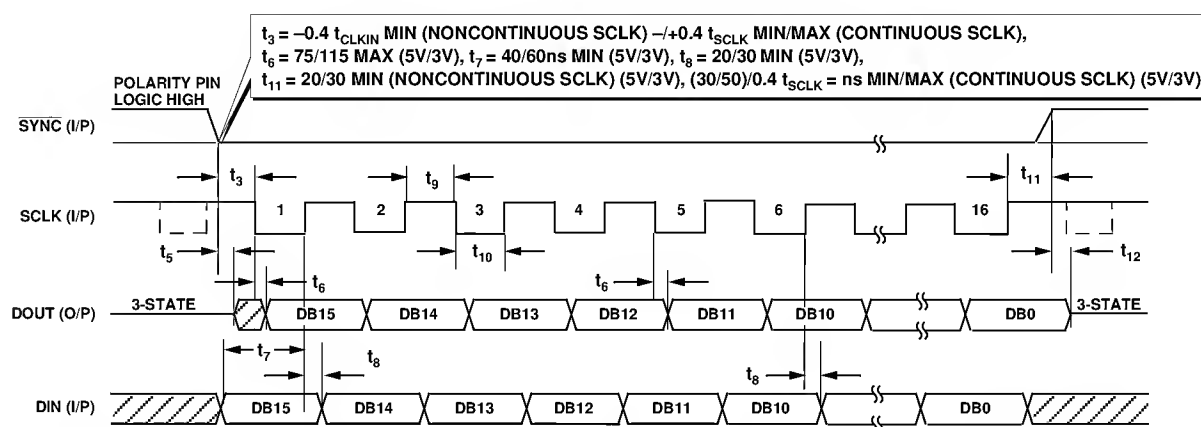


Figure 40. SPI/QSPI Mode 2 Timing Diagram for Read/Write Operation with DIN Input, DOUT Output and  $\overline{\text{SYNC}}$  Input ( $\text{SM1} = \text{SM2} = 0$ )

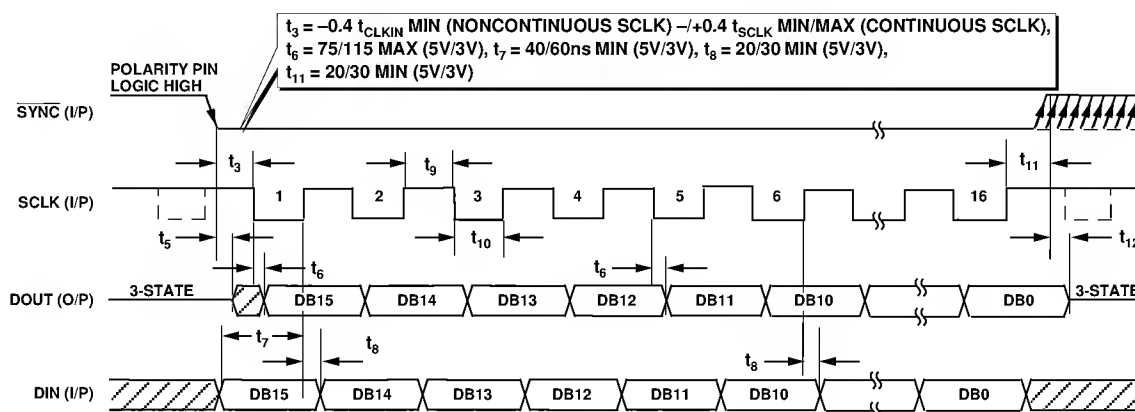


Figure 41. QSPI Mode 3 Timing Diagram for Read/Write Operation with  $\overline{\text{SYNC}}$  Input Edge Triggered ( $\text{SM1} = 0$ ,  $\text{SM2} = 1$ )

## AD7853/AD7853L

The most important point about these two modes of operation mode is that **the result of the current conversion is clocked out during the same conversion** and a write to the part during this conversion is for the next conversion. The arrangement is shown in Figure 42. Figure 43 and Figure 44 show more detailed timing for the arrangement of Figure 42.

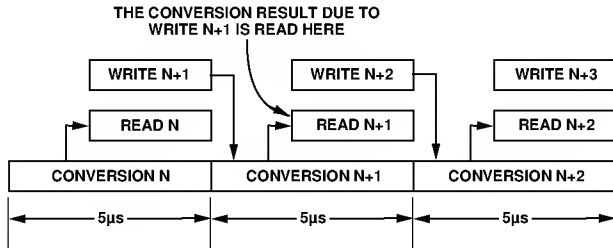


Figure 42.

In Figure 43 the first point to note is that the  $\overline{\text{BUSY}}$ ,  $\overline{\text{SYNC}}$ , and  $\text{SCLK}$  are all outputs from the AD7853/AD7853L with the  $\overline{\text{CONVST}}$  being the only input signal. Conversion is initiated with the  $\overline{\text{CONVST}}$  signal going low. This  $\overline{\text{CONVST}}$  falling edge also triggers the  $\overline{\text{BUSY}}$  to go high. The  $\overline{\text{CONVST}}$  signal rising edge triggers the  $\overline{\text{SYNC}}$  to go low after a short delay ( $0.5 t_{\text{CLKIN}}$  to  $1.5 t_{\text{CLKIN}}$  typically) after which the  $\text{SCLK}$  will clock out the data on the DOUT pin during conversion. The data on the DIN pin is also clocked in to the AD7853/AD7853L by the same  $\text{SCLK}$  for the next conversion. The read/write operations must be complete after sixteen clock cycles (which takes  $4.6 \mu\text{s}$  approximately from the rising edge of  $\overline{\text{CONVST}}$  assuming a  $4 \text{ MHz CLKIN}$ ). At this time the conversion will be complete, the  $\overline{\text{SYNC}}$  will go high, and the  $\overline{\text{BUSY}}$  will go low. The next falling edge of the  $\overline{\text{CONVST}}$  must occur at least 400 ns after the falling edge of  $\overline{\text{BUSY}}$  to allow the track/hold amplifier adequate acquisition time as shown in Figure 43. This gives a throughput time of  $5 \mu\text{s}$ . The maximum throughput rate in this case is 200 kHz (AD7853) and 100 kHz (AD7853L).

In these interface modes the part is now the master and the DSP is the slave. Figure 44 is an expansion of Figure 43. The AD7853/AD7853L will ensure  $\overline{\text{SYNC}}$  goes low after the rising edge C of the continuous  $\text{SCLK}$  (Interface Mode 5) in Figure 44. Only in the case of a noncontinuous  $\text{SCLK}$  (Interface Mode 4) will the time  $t_4$  apply. The first data bit is clocked out from the falling edge of  $\overline{\text{SYNC}}$ . The  $\text{SCLK}$  rising edge clocks out all

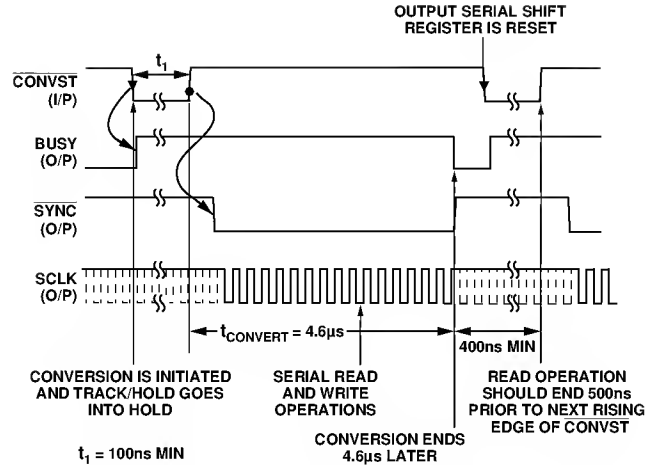


Figure 43. Mode 4, 5 Timing Diagram ( $\text{SM1} = 1$ ,  $\text{SM2} = 1$  and 0)

subsequent bits on the DOUT pin. The input data present on the DIN pin is clocked in on the rising edge of the  $\text{SCLK}$ . The POLARITY pin may be used to change the  $\text{SCLK}$  edge which the data is sampled on and clocked out on. The  $\overline{\text{SYNC}}$  will go high after the 16th  $\text{SCLK}$  rising edge and before the rising edge D of the continuous  $\text{SCLK}$  in Figure 44. This ensures the part will not clock in an extra bit from the DIN pin or clock out an extra bit on the DOUT pin.

If the user has control of the  $\overline{\text{CONVST}}$  pin but does not want to exercise it for every conversion, the control register may be used to start a conversion. Setting the  $\overline{\text{CONVST}}$  bit in the control register to 1 starts a conversion. If the user does not have control of the  $\overline{\text{CONVST}}$  pin, a conversion should not be initiated by writing to the control register. The reason for this is that the user may get “locked out” and not be able to perform any further write/read operations. When a conversion is started by writing to the control register, the  $\overline{\text{SYNC}}$  goes low and read/write operations take place while the conversion is in progress. However, once the conversion is complete, there is no way of writing to the part unless the  $\overline{\text{CONVST}}$  pin is exercised. The  $\overline{\text{CONVST}}$  signal triggers the  $\overline{\text{SYNC}}$  signal low which allows read/write operations to take place.  $\overline{\text{SYNC}}$  must be low to perform read/write operations. The  $\overline{\text{SYNC}}$  is triggered low by the  $\overline{\text{CONVST}}$  signal rising edge or setting the  $\overline{\text{CONVST}}$  bit in the control register to 1. Therefore if there is not full control of the  $\overline{\text{CONVST}}$  pin the user may end up getting “locked out.”

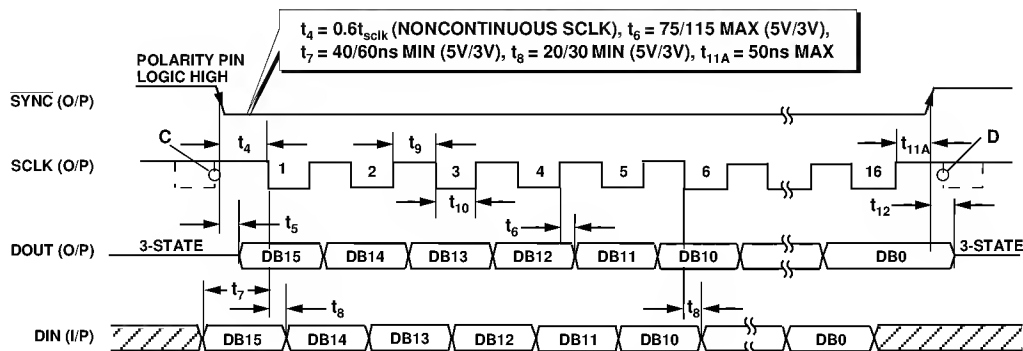


Figure 44. Timing Diagram for Read/Write with  $\overline{\text{SYNC}}$  Output and  $\text{SCLK}$  Output (Continuous and Noncontinuous) (i.e., Operating Mode Numbers 4 and 5,  $\text{SM1} = 1$ ,  $\text{SM2} = 1$  and 0)

## CONFIGURING THE AD7853/AD7853L

### AD7853/AD7853L as a Read-Only ADC

The AD7853/AD7853L contains fourteen on-chip registers which can be accessed via the serial interface. In the majority of applications it will not be necessary to access all of these registers. Figure 45 outlines a flowchart of the sequence which is used to configure the AD7853/AD7853L as a Read-Only ADC.

In this case there is no writing to the on-chip registers and only the conversion result data is read from the part. Interface Mode 1 cannot be used in this case as it is necessary to write to the control register to set Interface Mode 1. Here the CLKIN signal is applied directly after power-on, the CLKIN signal must be present to allow the part to perform a calibration. This automatic calibration will be completed approximately 150 ms after power-on.

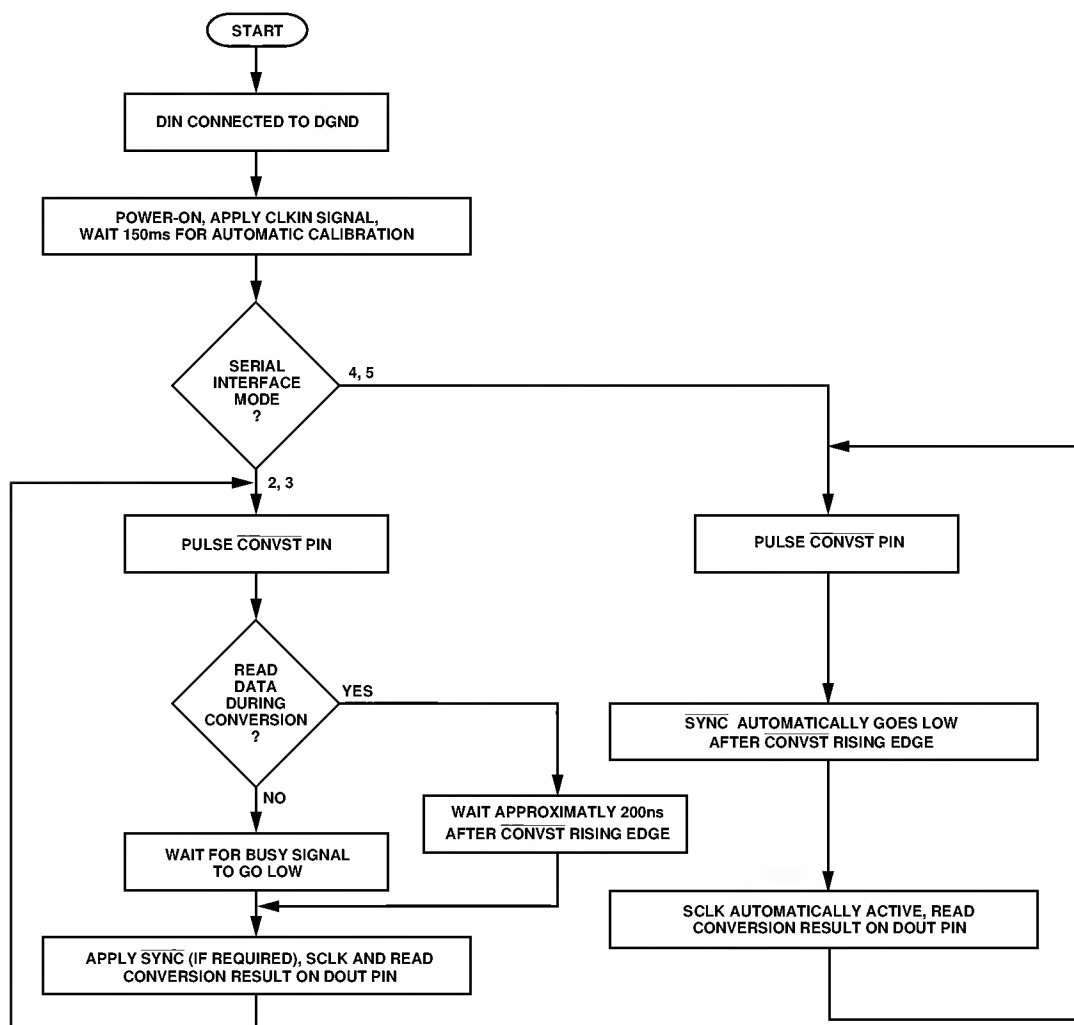


Figure 45. Flowchart for Setting Up and Reading from the AD7853/AD7853L

# AD7853/AD7853L

## Writing to the AD7853/AD7853L

For accessing the on-chip registers it is necessary to write to the part. To enable Serial Interface Mode 1, the user must also write to the part. Figure 46 through 48 outline flowcharts of how to configure the AD7853/AD7853L for each of the different serial interface modes. The continuous loops on all diagrams indicate the sequence for more than one conversion. The options of using a hardware (pulsing the CONVST pin) or software (setting the CONVST bit to 1) conversion start, and reading/writing during or after conversion are shown in Figures 46 and 47. If the  $\overline{\text{CONVST}}$  pin is never used then it should be tied to  $\text{DV}_{\text{DD}}$  permanently. Where reference is made to the

BUSY bit equal to a logic 0, to indicate the end of conversion, the user in this case would poll the BUSY bit in the status register.

## Interface Modes 2 and 3 Configuration

Figure 46 shows the flowchart for configuring the part in Interface Modes 2 and 3. For these interface modes, the read and write operations take place simultaneously via the serial port. Writing all 0s ensures that no valid data is written to any of the registers. When using the software conversion start and transferring data during conversion, Note must be obeyed.

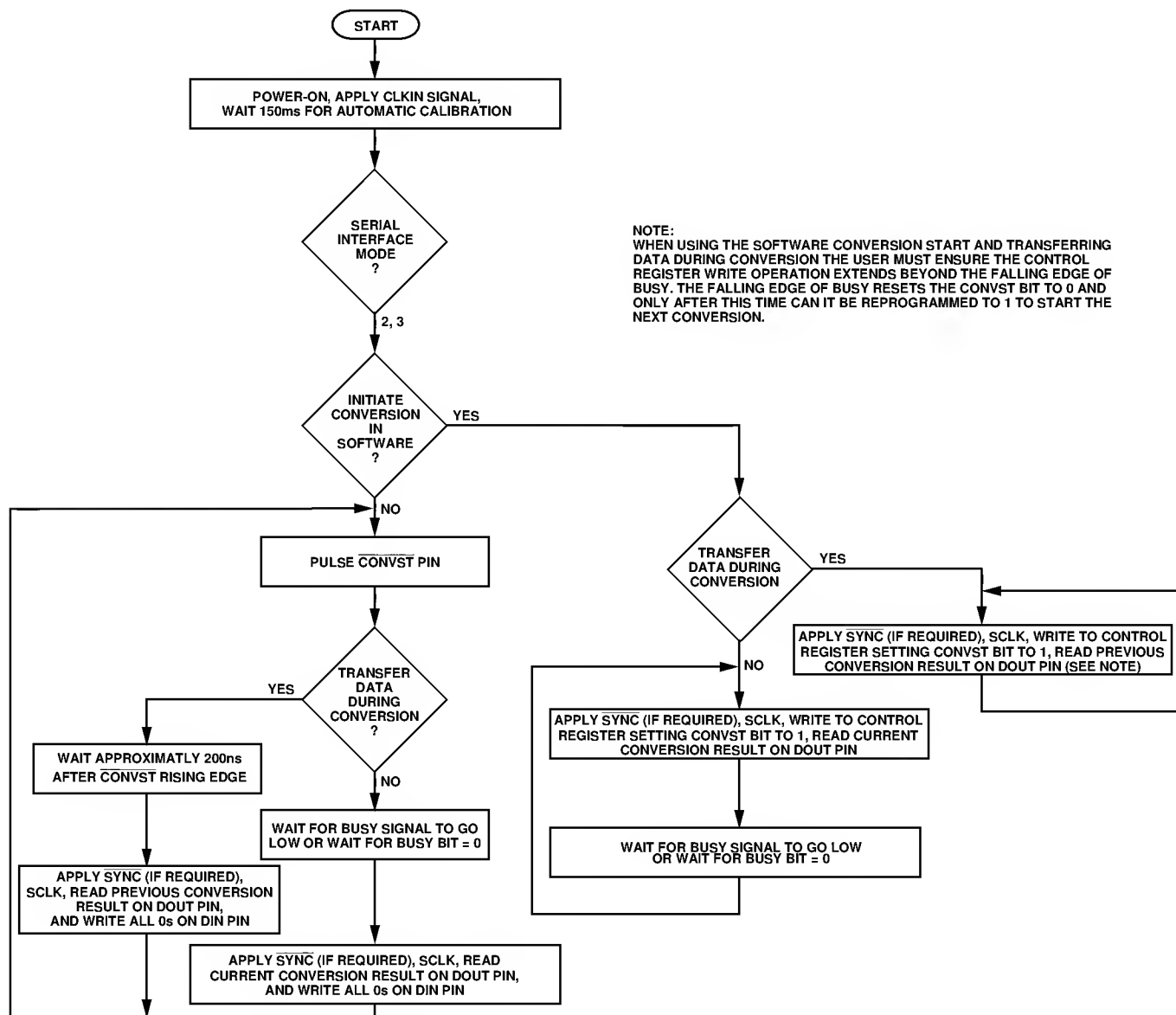


Figure 46. Flowchart for Setting Up, Reading, and Writing in Interface Modes 2 and 3

### Interface Mode 1 Configuration

Figure 47 shows the flowchart for configuring the part in Interface Mode 1. This mode of operation can only be enabled by writing to the control register and setting the  $2/3$  MODE bit. Reading and writing cannot take place simultaneously in this mode as the DIN pin is used for both reading and writing.

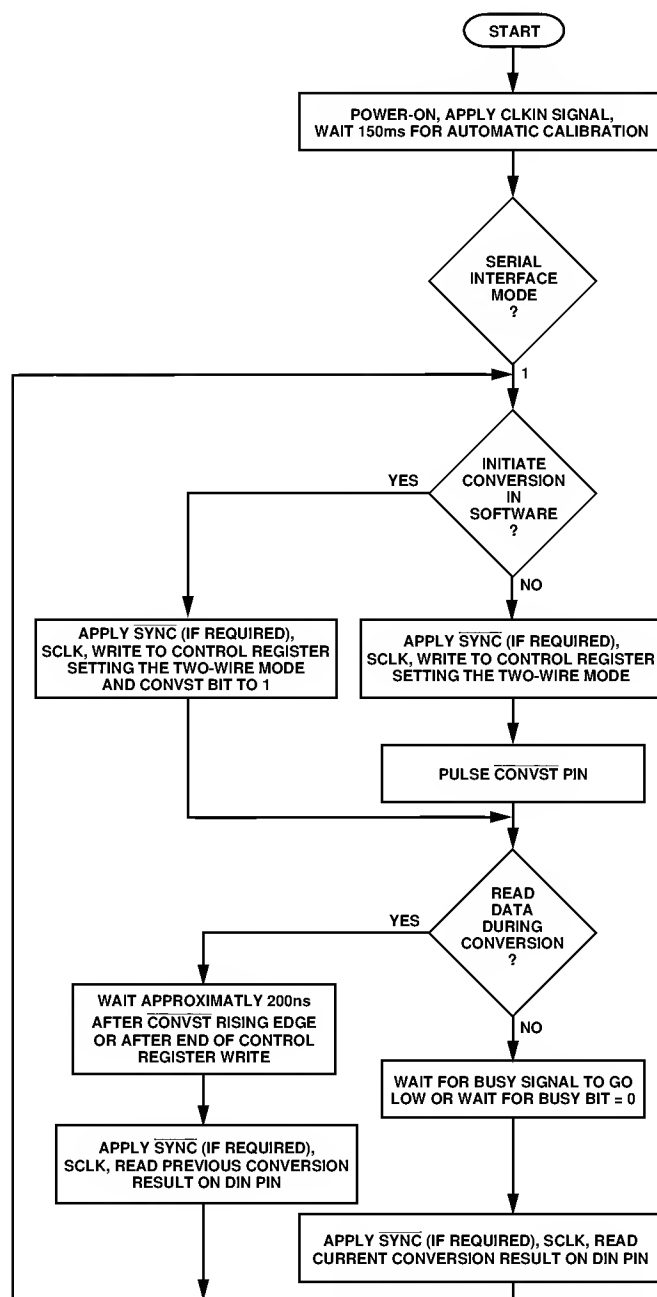


Figure 47. Flowchart for Setting Up, Reading, and Writing in Interface Mode 1

### Interface Modes 4 and 5 Configuration

Figure 48 shows the flowchart for configuring the AD7853/AD7853L in Interface Modes 4 and 5, the self-clocking modes. In this case it is not recommended to use the software conversion start option. The read and write operations always occur simultaneously and during conversion.

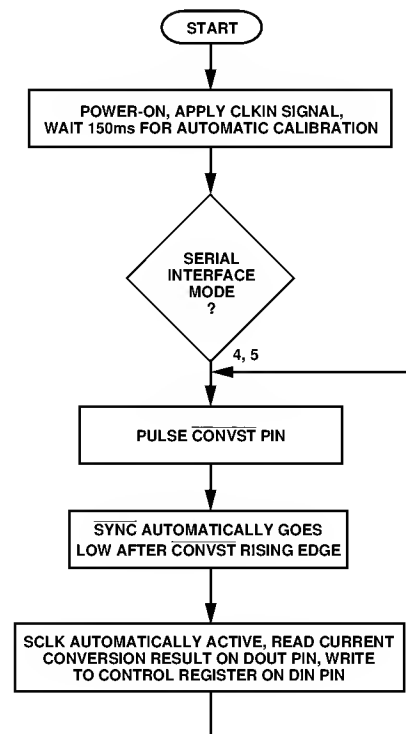


Figure 48. Flowchart for Setting Up, Reading, and Writing in Interface Modes 4 and 5

# AD7853/AD7853L

## MICROPROCESSOR INTERFACING

In many applications, the user may not require the facility of writing to the on-chip registers. The user may just want to hardwire the relevant pins to the appropriate levels and read the conversion result. In this case the DIN pin can be tied low so that the on-chip registers are never used. Now the part will operate as a nonprogrammable analog to digital converter where the  $\overline{\text{CONVST}}$  is applied, a conversion is performed and the result may be read using the SCLK to clock out the data from the output register on to the DOUT pin. Note that the DIN pin cannot be tied low when using the two-wire interface mode of operation.

The SCLK can also be connected to the CLKIN pin if the user does not want to have to provide separate serial and master clocks in Interface Modes 1, 2, and 3. With this arrangement the  $\overline{\text{SYNC}}$  signal must be low for 16 SCLK cycles in Interface Modes 1 and 2 for the read and write operations. For Interface Mode 3 the  $\overline{\text{SYNC}}$  can be low for more than 16 SCLK cycles for the read and write operations. Note that in Interface Modes 4 and 5 the CLKIN and SCLK cannot be tied together as the SCLK is an output and the CLKIN is an input.

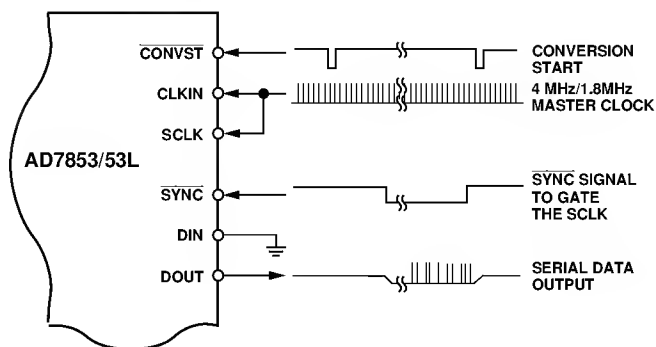


Figure 49. Simplified Interface Diagram with DIN Grounded and SCLK Tied to CLKIN

## AD7853/AD7853L to 8XC51/PIC17C42 Interface

Figure 50 shows the AD7853/AD7853L interface to the 8XC51/PIC17C42. The 8XL51 is for interfacing to the AD7853/AD7853L when the supply is at 3 V. The 8XC51/PIC17C42 only run at 5 V. The 8XC51 is in Mode 0 operation. This is a two-wire interface consisting of the SCLK and the DIN which acts as a bidirectional line. The  $\overline{\text{SYNC}}$  is tied low. The  $\overline{\text{BUSY}}$  line can be used to give an interrupt driven system but this would not normally be the case with the 8XC51/PIC17C42. For the 8XC51 12 MHz version, the serial clock will run at a maximum of 1 MHz so that the serial interface to the AD7853/AD7853L will only be running at 1 MHz. The CLKIN signal must be provided separately to the AD7853/AD7853L from a port line on the 8XC51 or from a source other than the 8XC51. Here the SCLK cannot be tied to the CLKIN as the 8XC51 only provides a noncontinuous serial clock. The  $\overline{\text{CONVST}}$  signal can be provided from an external timer or conversion can be started in software if required. The sequence of events would typically be writing to the control register via the

DIN line setting a conversion start and the 2-wire interface mode (this would be performed in two 8-bit writes), wait for the conversion to be finished ( $4.5\ \mu\text{s}$  with 4 MHz CLKIN), read the conversion result data on the DIN line (this would be performed in two 8-bit reads), and then repeat the sequence. The maximum serial frequency will be determined by the data access and hold times of the 8XC51/PIC16C42 and the AD7853/AD7853L.

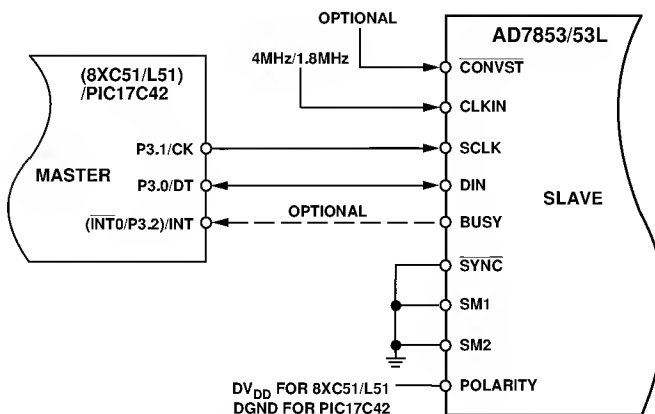


Figure 50. 8XC51/PIC16C42 Interface

## AD7853/AD7853L to 68HC11/16/L11 / PIC16C42 Interface

Figure 51 shows the AD7853/AD7853L SPI/QSPI interface to the 68HC11/16/L11/PIC16C42. The 68L11 is for interfacing to the AD7853/AD7853L when the supply is at 3 V. The  $\overline{\text{SYNC}}$  line is not used and is tied to DGND. The  $\mu\text{Controller}$  is configured as the master, by setting the MSTR bit in the SPCR to 1, and thus provides the serial clock on the SCK pin. For all the  $\mu\text{Controllers}$ , the CPOL bit is set to 1 and for the 68HC11/16/L11, the CPHA bit is set to 1. The CLKIN and  $\overline{\text{CONVST}}$  signals can be supplied from the  $\mu\text{Controller}$  or from separate sources. The  $\overline{\text{BUSY}}$  signal can be used as an interrupt to tell the  $\mu\text{Controller}$  when the conversion is finished, then the reading and writing can take place. If required the reading and writing can take place during conversion and there will be no need for the  $\overline{\text{BUSY}}$  signal in this case. For no writing to the part then the DIN pin can be tied permanently low. For the 68HC16 and the QSPI interface the SM2 pin should be tied high and the  $\overline{\text{SS}}$  line tied to the  $\overline{\text{SYNC}}$  pin. The microsequencer on the 68HC16 QSPI port can be used for performing a number of read and write operations independent of the CPU and storing the conversion results in memory without taxing the CPU. The typical sequence of events would be writing to the control register via the DIN line setting a conversion start and at the same time reading data from the previous conversion on the DOUT line, wait for the conversion to be finished ( $4.5\ \mu\text{s}$  with 4 MHz CLKIN), and then repeat the sequence. The maximum serial frequency will be determined by the data access and hold times of the  $\mu\text{Controllers}$  and the AD7853/AD7853L.



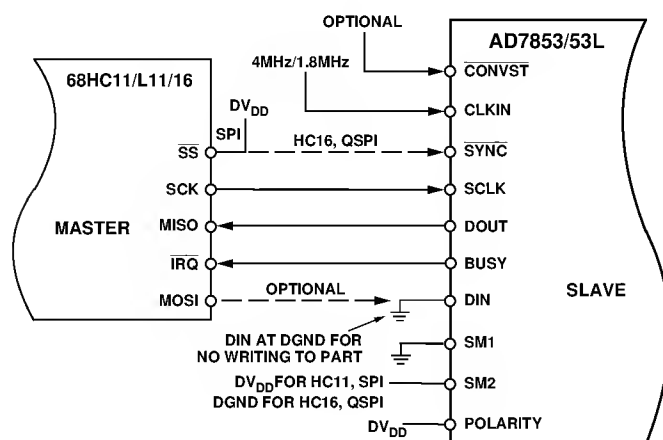


Figure 51. 68HC11 and 68HC16 Interface

## AD7853/AD7853L to ADSP-21xx Interface

Figure 52 shows the AD7853/AD7853L interface to the ADSP-21xx. The ADSP-21xx is the slave and the AD7853/AD7853L is the master. The AD7853/AD7853L is in Interface Mode 5. For the ADSP-21xx, the bits in the serial port control register should be set up as TFSR = RFSR = 1 (need a frame sync for every transfer), SLEN = 15 (16-bit word length), TFSW = RFSW = 1 (alternate framing mode for transmit and receive operations), INVRFS = INVTFS = 1 (active low RFS and TFS), IRFS = ITFS = 0 (External RFS and TFS), and ISCLK = 0 (external serial clock). The CLKIN and CONVST signals could be supplied from the ADSP-21xx or from an external source. The AD7853/AD7853L supplies the SCLK and the SYNC signals to the ADSP-21xx and the reading and writing takes place during conversion. The BUSY signal only indicates when the conversion is finished and may not be required. The data access and hold times of the ADSP-21xx and the AD7853/AD7853L allows for a CLKIN of 4 MHz/1.8 MHz at both 5 V and 3 V supplies.

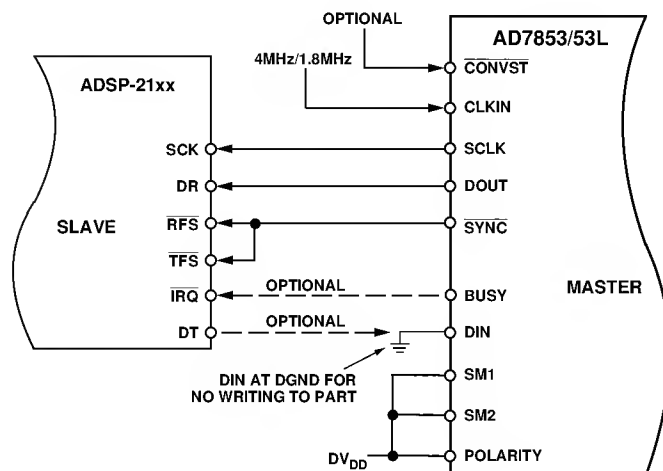


Figure 52. ADSP-21xx Interface

## AD7853/AD7853L to DSP56000/1/2/L002 Interface

Figure 53 shows the AD7853/AD7853L to DSP56000/1/2/L002 interface. Here the DSP5600x is the master and the AD7853/AD7853L is the slave. The AD7853/AD7853L is in Interface Mode 3. The DSP56L002 is used when the AD7853/AD7853L is being operated at 3 V. The setting of the bits in

the registers of the DSP5600x would be for synchronous operation (SYN = 1), internal frame sync (SCD2 = 1), Internal clock (SCKD = 1), 16-bit word length (WL1 = 1, WL0 = 0), frames sync only active at beginning of the transfer (FSL1 = 0, FSL0 = 1). A gated clock can be used (GCK = 1) or if the SCLK is to be tied to the CLKIN of the AD7853/AD7853L, then there must be a continuous clock (GCK = 0). Again the data access and hold times of the DSP5600x and the AD7853/AD7853L should allow for an SCLK of 4 MHz/1.8 MHz.

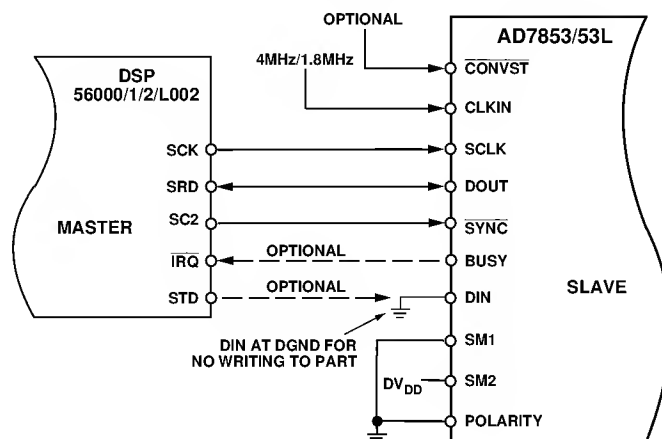


Figure 53. DSP56000/1/2 Interface

## AD7853/AD7853L to TMS320C20/25/5x/LC5x Interface

Figure 54 shows the AD7853/AD7853L to the TMS320Cxx interface. The TMS320LC5x is used when the AD7853/AD7853L is being operated at 3 V. The AD7853/AD7853L is the master and operates in Interface Mode 5. For the TMS320Cxx the CLKX, CLKR, FSX, and FSR pins should all be configured as inputs. The CLKX and the CLKR should be connected together as should the FSX and FSR. Since the AD7853/AD7853L is the master and the reading and writing occurs during the conversion, the BUSY only indicates when the conversion is finished and thus may not be required. Again the data access and hold times of the TMS320Cxx and the AD7853/AD7853L allows for a CLKIN of 4 MHz/1.8 MHz.

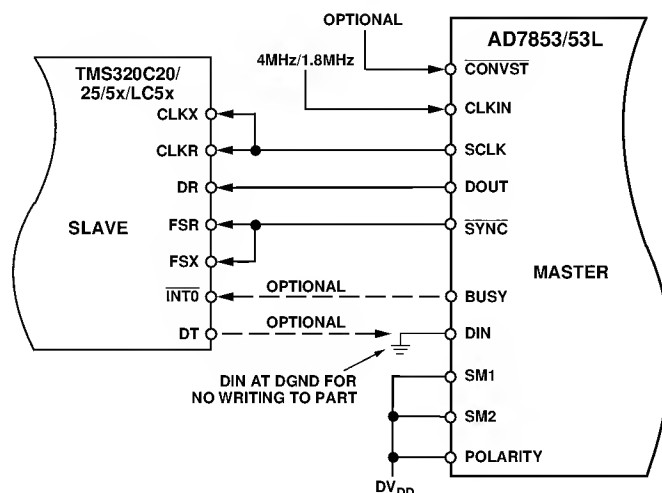


Figure 54. TMS320C20/25/5x Interface

# AD7853/AD7853L

## APPLICATION HINTS

### Grounding and Layout

The analog and digital supplies to the AD7853/AD7853L are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The part has very good immunity to noise on the power supplies as can be seen by the PSRR versus Frequency graph. However, care should still be taken with regard to grounding and layout.

The printed circuit board that houses the AD7853/AD7853L should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7853/AD7853L is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7853/AD7853L. If the AD7853/AD7853L is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7853/AD7853L.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7853/AD7853L to avoid noise coupling. The power supply lines to the AD7853/AD7853L should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10  $\mu\text{F}$  tantalum in parallel with 0.1  $\mu\text{F}$  capacitors to AGND. All digital supplies should have a 0.1  $\mu\text{F}$  disc ceramic capacitor to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. In systems where a common supply voltage is used to drive both the  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  of the AD7853/AD7853L, it is recommended that the system's  $\text{AV}_{\text{DD}}$  supply is used. In this case there should be a 10  $\Omega$  resistor between the  $\text{AV}_{\text{DD}}$  pin and  $\text{DV}_{\text{DD}}$  pin. This supply should have the recommended analog supply decoupling capacitors between the  $\text{AV}_{\text{DD}}$  pin of the AD7853/AD7853L and AGND and the recommended digital supply decoupling capacitor between the  $\text{DV}_{\text{DD}}$  pin of the AD7853/AD7853L and DGND.

### Evaluating the AD7853/AD7853L Performance

The recommended layout for the AD7853/AD7853L is outlined in the evaluation board for the AD7853/AD7853L. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7853/AD7853L Evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7853/AD7853L.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7853/AD7853L. It also gives full access to all the AD7853/AD7853L on-chip registers allowing for various calibration and power-down options to be programmed.

### AD785x Family

All parts are 12 bits, 200 kSPS, 3.0 V to 5.5 V.

### AD7853 – Single Channel Serial

### AD7854 – Single Channel Parallel

### AD7858 – Eight Channel Serial

### AD7859 – Eight Channel Parallel

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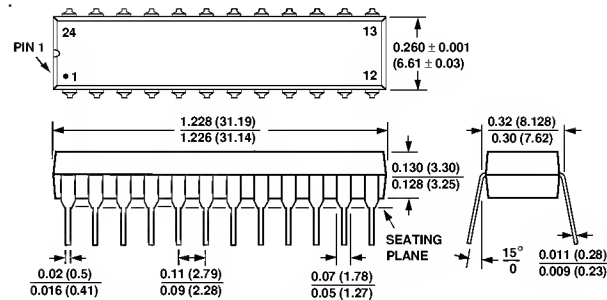
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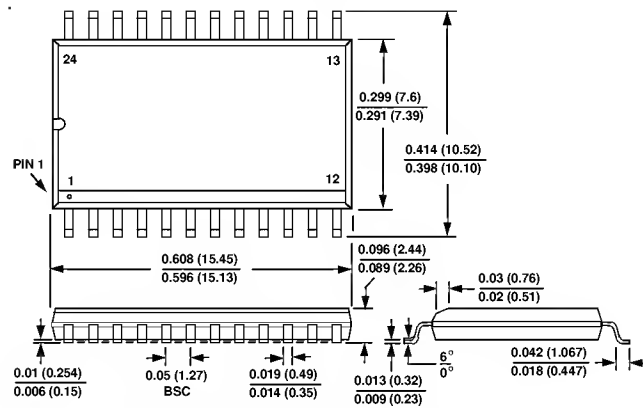
OUTLINE DIMENSIONS  
Dimensions shown in inches and (mm).

24-Pin Plastic DIP  
(N-24)



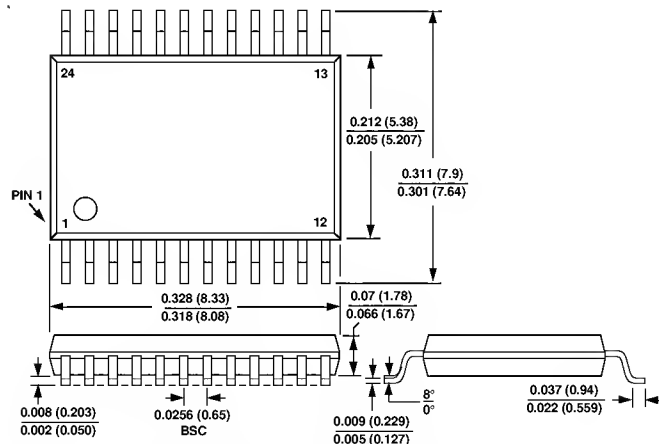
- NOTES  
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH  
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN PLATED  
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Small Outline Package  
(R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.  
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED  
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

24-Pin Shrink Small Outline Package  
(RS-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.  
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED  
IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS